Kowsyap Pranay Kumar Musumuri

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Experience

Graduate Teaching Assistant | George Mason University Jan 2025 – Present | VA, USA
- Supported coursework in **computer architecture**, **memory organization**, **control design**, and **digital system design** using HDL languages.
- Streamlined **FPGA** design flow and implemented hardware solutions.

Power Programmer | Infosys Nov 2023 – Jul 2024 | HYD, India
- Developed a **research** based web application for **Ingredion**, enhancing recipe and material management with intuitive interfaces and efficient backend design, ensured secure and scalable deployment on **Azure**.
- Engineered dynamic UIs with **Angular**, **ReactJS**, and **RxJS**, improving user experience and boosting site interaction by **30%.**
- Created robust **RESTful APIs** and **GraphQL** endpoints using NodeJS, optimized MongoDB schemas and queries.
- Harnessed **Python** and **ML** frameworks to develop predictive models, enhancing process optimization by **15%.**

Software Engineer | MSR Cosmos LLC May 2021 – Nov 2023 | HYD, India
- Leveraged **2.5 years** of experience to develop and refine complex applications for **TMILL** and **Vinci360**, boosting operational efficiency and delivering critical social media insights.
- Created impactful internal tools using Java, NodeJS, Angular, and related technologies, enhancing workflow and efficiency.
- Mentored 5+ team members and drove successful collaboration on projects.
- Built and deployed **CI/CD pipelines** in **Azure DevOps**, automating code integration and delivery processes

Embedded Linux Project Lead Intern | IoTIoT.in Jul 2020 – Jan 2021 | PUN, India
- Spearheaded the design and implementation of a real-time research **AIoT** solution, titled **Transformer Anomaly Detector**
- Delivered an industry-ready product engineered to detect and predict anomalies in transformers with **95%** precision, utilizing **Python**, **TensorFlow**, and **Raspberry Pi** to enhance operational efficiency and minimizing downtime in industrial environments.

Design and Verification Intern | SION Semiconductors Pvt Ltd May 2020 – Nov 2020 | BAN, India
- Mastered **SoC design** and **verification** methodologies, utilizing **SystemVerilog** and **UVM** environments.
- Engineered and validated **Dual Ported RAM** and **APB** protocols, demonstrating hands-on proficiency in advanced verification techniques.

Education

George Mason University Aug 2024 – Present | Virginia, USA
Master of Science in Computer Engineering | GPA: 3.89/4.0

Indian Institute of Information Technology Jul 2017 – May 2021 | Kurnool, India
Bachelor of Technology in Electronics Engineering | GPA: 8.77/10.0

Skills

Hardware Description Languages: Verilog, VHDL, SystemVerilog, UVM

Programming Languages: C, C++, Python, Java, JavaScript, TypeScript, PHP, C#, Bash

Embedded Systems: Embedded C, Real-Time Operating Systems (RTOS), x86 Assembly, 8051 Assembly

Web Technologies: Angular, ReactJS, NodeJs, ExpressJS

Databases: MongoDB, MySQL, PostgreSQL

Operating Systems: Linux, Windows, MacOS

Machine Learning & Data Analysis: Pandas, NumPy, Scikit-learn, TensorFlow

Software & Tools: Cadence, Xilinx Vivado, QuestaSim, AutoCAD, MATLAB, Octave, LabVIEW, Git, Azure

Coursework/Experience: Digital System Design, Computer Architecture, CMOS Design, Data Structures & Algorithms

Projects

Hardware Implementation of Signature Verification in New Post-Quantum Signature Scheme MAYO (*Xilinx Vivado*, *VHDL*, *C*, *JS)*

8 bit Harvard Architecture based Processor (*Verilog*, *Xilinx Vivado*)

Memory Level Design and Verification of DPRAM (*SystemVerilog*, *UVM*, *QuestaSim*)

Transformer Anomaly Detection (Python, *Lazypredict*, *Random Forests*, *Raspberry Pi*)

Ng-dyno-form : Dynamic Customizable Reactive Form (*Angular*, *RxJS*, *Reactive Forms*)

Publications

Correctness of Synthesis for Tree based Decomposed Algorithm in Semiconductor Memory Designs with Larger Decoders, IEEE 2021

Certificates

- Azure Fundamentals
- Azure AI Fundamentals
- Azure Data Fundamentals
- Machine Learning
- Programming the IoT
- HDL for FPGA Design