



FOBOS 3: an open-source platform for side-channel analysis and benchmarking

Eduardo Ferrufino¹ · Luke Beckwith¹ · Abubakr Abdulgadir² · Jens-Peter Kaps¹

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Abstract

The lightweight cryptography (LWC) standardization process by the National Institute of Standards and Technology (NIST) of the US is the latest example of competitions that require benchmarking and side-channel leakage evaluation of hardware and software implementations of a multitude of candidate algorithms. A common hardware application programming interface (API) streamlines the development of a test harness. However, no existing platform is directly compatible with the LWC algorithms' hardware interface. Hence, a significant effort is needed to evaluate and benchmark a large number of candidates. This paper presents an open-source, multi-user platform for side-channel analysis and benchmarking we call FOBOS 3. It contains its own measurement board (FOBOS Shield), target board (FBD-A7 with Xilinx Artix-7-A12 FPGA), and Multi-Target Connector (MTC) to use microcontroller boards from Texas Instruments and ST Microelectronics. It enables side-channel leakage evaluation as well as measurement of power and energy consumption on both: FPGA and microcontroller targets. Case studies are included to highlight these features.

Keywords Side-channel analysis · Benchmarking · Hardware security · Lightweight cryptography

1 Introduction

Security evaluation and benchmarking of cryptographic implementations are crucial phases in designing solutions capable of successful deployment. Side-channel attacks [15] pose a severe threat to the security of cryptographic functions, which lie at the core of security mechanisms protecting valuable data.

However, implementing side-channel-resistant cryptographic functions is a complex and error-prone process. Hence, validation steps must be performed to ensure that the design meets the intended security goals. Validation can take the form of mounting attacks at various attack points

or performing statistical leakage assessments such as Test Vector Leakage Assessment (TVLA) [8, 28].

Power and energy consumption are also vital considerations, especially for battery-powered devices. Hence, they should be accurately measured to ensure the design is within the power and energy budgets for the application in mind.

Tools for performing security evaluation and benchmarking are already available and range from high-end and costly commercial equipment to ad-hoc setups built for a single experiment. However, in some situations, low-cost, highly accessible, and flexible tools are needed. This is where we see a gap in currently used platforms.

At the ASHES'23 workshop in Copenhagen [7], we presented a significantly updated version of the FOBOS side-channel analysis platform with applications in research and education. This includes a new control board with an internal ADC capable of measuring traces using a sampling clock synchronous to the target clock, providing precise measurements. Additionally, the control board can measure the target's power consumption. We also introduce a new low-cost FPGA-based target board, providing another option for evaluating hardware designs. Furthermore, we presented case studies illustrating the effectiveness of our platform in the

✉ Jens-Peter Kaps
jkaps@gmu.edu

Eduardo Ferrufino
eferruf@gmu.edu

Luke Beckwith
lbeckwit@gmu.edu

Abubakr Abdulgadir
abubakr.abdulgadir@pqsecurity.com

¹ George Mason University, Fairfax, VA, USA

² PQSecure Technologies, Boca Raton, FL, USA

security evaluation and benchmarking of finalists in the NIST lightweight cryptography standardization process.

In this work, we expanded FOBOS 3 with a Multi-Target Connector (MTC) to provide connectivity to readily available microcontroller boards from Texas Instruments (TI) and ST Microelectronics (STM). We added the I2C bus to FOBOS for communication with microcontrollers and updated the protocol FOBOS uses to interface with devices under test. Furthermore, we developed a new FOBOS Shield for the Pynq-Z2 board.

Hence, we claim the following contribution:

- (1) An upgraded side-channel analysis platform capable of mounting attacks, assessing leakage, and performing power measurements. The platform is open-source, enabling result replication and further improvement by the community.
- (2) A new target board based on a small low-cost FPGA.
- (3) A Multi-Target Connector board to interface with TI Launchpads and STM Nucleo boards.
- (4) Comparison of leakage assessment results of a protected implementation of the NIST LWC finalist Xoodoo using synchronous and asynchronous sampling.
- (5) Comparison of power consumption measurements of the NIST LWC winner Ascon on two different FPGA boards with estimates generated by simulation.
- (6) Description of differential power analysis of AES on a TI MSP430 microcontroller.

2 Previous work

Several side-channel and benchmarking platforms are available and widely used in the cryptographic community. The Rambus DPA Workstation [25] and Riscure Inspector [26] are examples of commercial platforms. The SASEBO [13] and the SAKURA boards [9] have been used in many academic publications and provide FPGA and smart-card targets. The NewAE ChipWhisperer is an open-source platform widely used in academia and industry and provides target boards for microcontrollers and FPGAs. ChipWhisperers sampling clock can be synchronized with the target clock enabling more precise measurements [21].

FOBOS, which stands for “Flexible Opensource work-Bench fOr Side-channel analysis” and is loosely named after the Greek god Phobos ($\phi\acute{o}\beta\omicron\varsigma$) who personifies fear and can pierce shields, was first presented in the “Work in Progress” session of COSADE 2012 [31]. Unlike the SAKURA, it de-couples the control device from the Device Under Test (DUT), also called *target*. It uses off-the-shelf FPGA boards as control and modified DUTs along with custom-built boards. Version 2 of FOBOS, presented at ReConFig [1] in December 2019, replaces the monolithic control logic design

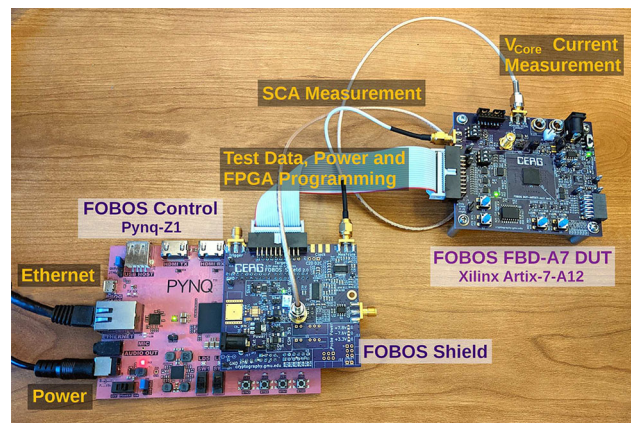


Fig. 1 FOBOS 3 setup with FOBOS Artix-7-A12 DUT

with a more flexible design based on functional modules and a Xilinx MicroBlaze processor. It provides a simple wrapper for FPGA implementations of cryptographic algorithms according to the CAESAR [10] and LWC Hardware API [12], which uses a FIFO-based approach. Additionally, FOBOS provides a simple Control-DUT protocol. Hence, we chose FOBOS 2 as the basis for our work.

3 FOBOS 3

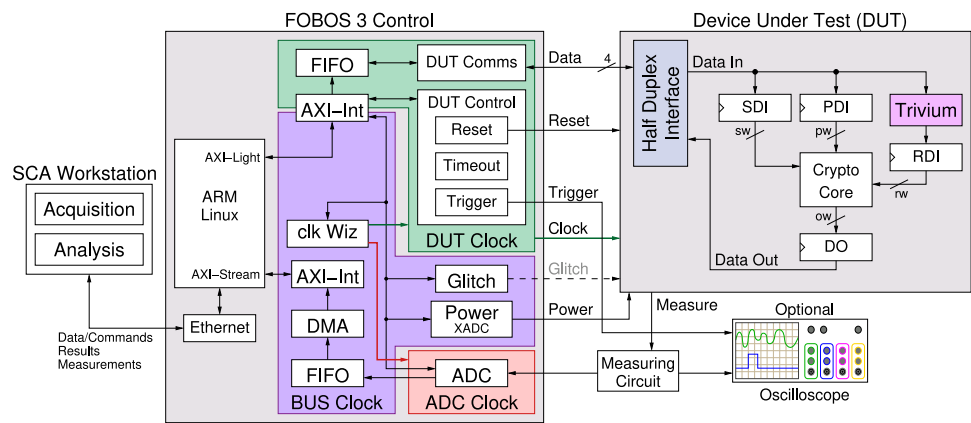
In order to develop an efficient multi-user platform for side-channel analysis and benchmarking, several drawbacks of the FOBOS 2 platform had to be overcome. The main drawback is that FOBOS 2 uses an external oscilloscope which increases the setup cost. Synchronous sampling is only possible with advanced oscilloscopes that allow for an external reference clock. Furthermore, FOBOS 2 has no built-in capability to perform power consumption measurements and uses USB/UART communication which leads to a low data transfer speed and it lacks multi-user capability. To address these drawbacks, we performed a major update to the FOBOS 2 platform resulting in the FOBOS 3 platform that we discuss in detail in this paper.

3.1 Platform overview

The main components of the FOBOS 3 platform are as follows:

- (1) The *SCA Workstation* hosts capture and analysis scripts. In typical system usage, the user interacts with Jupyter notebooks to run capture scripts that send test vectors (e.g., key and plaintext) one at a time to the connected control board and receive the results (e.g., ciphertext) and power traces. Analysis scripts can be run on the saved

Fig. 2 Block Diagram of FOBOS 3 with a Hardware DUT



results and traces or optionally executed simultaneously with trace collection.

- (2) The *control board* receives a test vector from the SCA workstation and forwards it to the DUT. The control board asserts a trigger signal as soon as the DUT starts operating on the test vector (i.e., running the cryptographic function). This signal can trigger an external oscilloscope or the internal ADC hosted in the FOBOS Shield, which we will discuss in Sect. 3.3. The control board also generates the target clock. The internal ADC can sample changes in the power consumption of the DUT at a maximum rate of 100M Sample/sec. The sampling clock and the target clocks are synchronized to achieve high-precision measurements.
- (3) The *DUT board* hosts the cryptographic function that is being evaluated. This board is designed (or modified) to allow measurement of the power consumption using a shunt resistor or a current probe. We tested the platform using a modified Digilent Nexys 3 board featuring a Xilinx Spartan-6 FPGA, the NewAE CW305 Artix-7 target board, our FOBOS Artix-7-based DUT board that is discussed in Sect. 5, and TIs MSP430FR6989 Launchpad via the new FOBOS MTC as presented in Sect. 6.3.

A typical FOBOS 3 setup is shown in Fig. 1. The control board is based on the PYNQ-Z1 board, which features a Xilinx Zynq-7020 system-on-chip with a dual-core ARM processor running Linux and tightly coupled with an FPGA fabric. We chose the PYNQ boards for FOBOS 3 as it has more flexibility and performance than a softcore processor or hardcoded logic. Furthermore, it supports segmentation of the control logic into software and hardware and its AXI bus allows us to re-use IP cores from FOBOS 2.

The custom FOBOS Shield is mounted on top of the PYNQ board and provides a 10-bit ADC, a pre-amplifier, power regulators, power measurement circuitry, and a target communication interface. We chose to develop shields for PYNQ-Z1 and PYNQ-Z2 rather than a capture board com-

plete with Zynq chip for simplicity. The target device shown in Fig. 1 on the right is the FOBOS Artix-7-A12 DUT.

The high-level block diagram of the FOBOS 3 system shown in Fig. 2 details the modules we built into the programmable logic on the Zynq chip. This includes modules to control and interact with the hardware of the FOBOS Shield. At the center is a clock wizard that generates the clock signals for the DUT (DUT Clock) and the ADC (ADC Clock) and ensures synchronization. The power module controls the power regulators and uses the Xilinx ADC (XADC) of the Zynq chip to measure output voltages and currents. The DUT control module provides triggering, among other tasks, while the DUT communications module handles the communication with the DUT. The control board is connected to the SCA workstation using a Gigabit Ethernet port to ensure high-speed data transfer.

On the target board, we provide flexible wrappers that provide translation from the FOBOS DUT Protocol, described in Sect. 3.4, to the Crypto Core Interface for both, hardware and software implementations of cryptographic algorithms. The Crypto Core interface for hardware implementations is compatible with the interfaces described in the CAESAR Hardware API [10] and the Hardware API for Lightweight Cryptography [12]. The wrapper receives data from the control board and distributes it to input FIFOs: SDI (secret data input) to store keys, PDI (public data input) for data such as plaintext. Optionally, random bits needed for masked implementations can be produced in the target FPGA using the provided Trivium-based [6] random number generator with a seed and provided via the RDI (random data input).

The Crypto Core interface for software implementations is compatible with the *Implementation Requirements for AEAD algorithms* set forth by NIST as submission requirements for the LWC standardization process [20] which are similar to the API used by SUPERCOP [3]. Here the wrapper stores the received data from the control board in arrays and provides pointers to them to the Crypto Core.

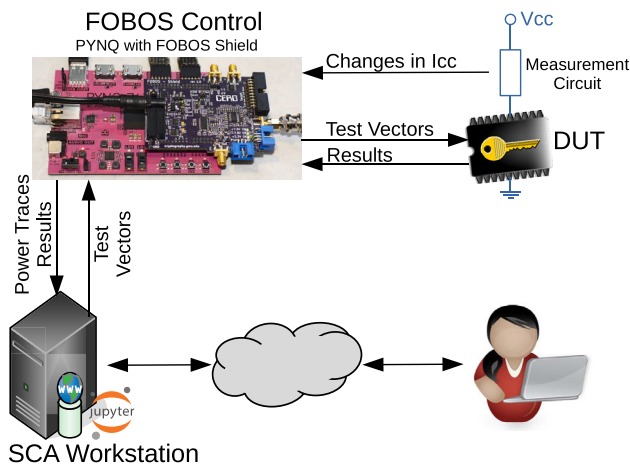


Fig. 3 FOBOS 3 setup with CW305 Artix-7-A100 DUT

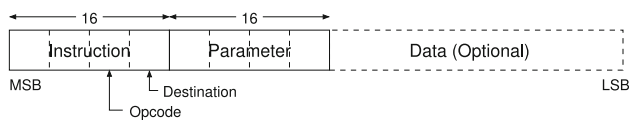


Fig. 4 Remote Access to FOBOS 3

Once data is stored in the input FIFOs or arrays, the wrapper allows the Crypto Core to run and consume their data. During the operation of the cryptographic function, all I/Os except for the clock are idle to minimize noise. The wrapper accumulates the output in the data output FIFO or array (DO) and sends it back to the control board after the Crypto Core finishes its execution.

3.2 Online access and application to teaching

We use JupyterLab, an interactive web-based development environment, to provide access to FOBOS. JupyterLab is hosted on the SCA Workstation and communicates with a server program on the FOBOS control board. The protocol allows the sending of commands, test vectors, and FPGA configuration data for the FOBOS DUT and the receiving of the power traces from the ADC, power consumption data, as well as results from the DUT. Figure 3 shows how FOBOS can be accessed remotely. All functions a user needs to interact with FOBOS are provided in a Python library (foboslib) including functions to handle multiple user requests for the same FOBOS setup. When a FOBOS setup is idle, a user can get exclusive access to configure the setup, program the DUT, and run measurements, after which the user should relinquish the access. In case the DUT becomes unresponsive, e.g., through glitching, or the user is idle for a long time, access is rescinded and the setup is brought back to a default state. This type of online access is not meant to offer SCA as a service to a wide audience, but to allow groups of peo-

ple to run their experiments from home and to easily share equipment.

We started using an early version of FOBOS 3 for online labs in an undergraduate university course in the Spring of 2020 when COVID19 forced a shutdown of in-person classes at our university. Our experience with using online SCA labs in the subsequent years has been described in [2].

3.3 FOBOS shield

We developed two versions of the FOBOS Shield with identical functionality, one plugs into the Arduino/chipKIT connector of the PYNQ-Z1 board, and the other into the Arduino and Raspberry Pi connectors of the PYNQ-Z2 board. The FOBOS Shield contains a version of the OpenADC [19] with a 10-bit ADC with 105 MS/s sampling rate and a software adjustable Low Noise Amplifier (LNA) with a gain of up to 55 dB and 40 MHz bandwidth. This is the same circuit used by ChipWhisperer-Lite. The ADC captures changes in power consumption or EM radiation of the target device. Communication and clocking of the target device is achieved through a 20-pin target connector, (see Table 1) which is compatible with ChipWhisperer target boards, and provides additional functionality such as programming the FPGA of our FOBOS Artix-7-A12 DUT.

The FOBOS Shield also contains a simple crow-bar voltage glitching circuit and outputs for clock and trigger signals on SMA connectors. Furthermore, it has an optional isolated probe power supply which can provide power for the NewAE CW501 differential probe and the NewAE CW502 low noise amplifier. In order to facilitate power consumption measurements for benchmarking, the FOBOS Shield contains three power supplies that allow calibrated voltage and current measurements. They are described in Sect. 3.5.

3.4 FOBOS DUT protocol

FOBOS uses the simple protocol to interface with a DUT shown in Fig. 4. An instruction consists of an *Opcode* and a *Destination*. The *Opcode* describes the type of storage to be used. Opcode $0xC$ indicates that multiple bytes of data are going to be sent. A hardware implementation, e.g. on an FPGA, would store this data in FIFO, and a software implementation, e.g. on a microcontroller, would store the data in an array. Opcode $0x8$ indicates that a single 16-bit word is going to be sent. That would be stored in a register. The *Opcode* is immediately followed by the *Destination*, i.e., the FIFO/array or register number. Each instruction is followed by a *Parameter*. In the case of FIFO/array destination, the parameter contains the number of bytes of data to be written. In the case of a register, it contains the data to be stored in the selected register.

Table 1 FOBOS Target Connector Pinout

Pin	Net	Comment	Pin	Net	Comment
1	FC_5V	5 V Supply	11	FC2D_HS	Handshaking Ctrl→DUT
2	GND		12	FC_DIO1	Data Bus bit 1
3	FC_3V3	3.3 V Supply	13	FD2C_HS	Handshaking DUT→Ctrl
4	FD2C_CLK	Clock DUT→Ctrl	14	FC_DIO2	Data Bus bit 2
5	FC_RST	DUT Reset	15	FC_PROG	Programming DUT
6	FC2D_CLK	Clock Ctrl→DUT	16	FC_DIO3	Data Bus bit 3
7	FC_IO	Direction of Bus	17	GND	
8	FD_VREF	IO Voltage of DUT	18	FC_3V3	3.3 V Supply
9	FD_TF	DUT Busy	19	GND	
10	FC_DIO0	Data Bus bit 0	20	FC_5V	5 V Supply

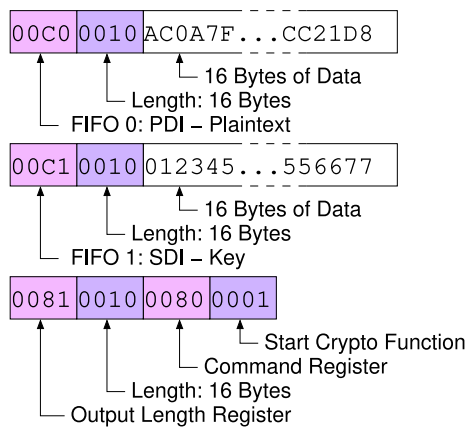


Fig. 5 FOBOS DUT Protocol

FOBOS supports up to 4 FIFOs and 8 Registers. FIFOs 0 and 1 are used for PDI and SDI. FIFOs 2 and 3, typically used for Associated Data (AD) and Nonce respectively, are optional as they are not used by all cryptographic functions. Additionally, the GMU LWC Hardware API for AEAD ciphers does not require these FIFOs as both AD and Nonce, are part of the test vector transmitted using the PDI FIFO.

Register 0 is the command register. It instructs the DUT to reset the PRNG, to tell the PRNG to generate new random numbers, or to start the crypto core. Register 1 contains the number of bytes expected from the crypto core, i.e., the output length. Register 3 contains user-definable bits that can be used for out-of-band signaling to the crypto core. Register 2 tells the PRNG how many bytes of random data to produce, and registers 4-7 store PRNG seed.

Figure 5 shows an example of a test vector for a block cipher. First, 128-bits (16 Bytes) plaintext are sent to FIFO-0, then 128-bits (16 Bytes) key is sent to FIFO-2, followed by the expected ciphertext length of 128-bit (16 Bytes) and the command to start encryption. Note that this test vector is independent of the actual AES implementation including

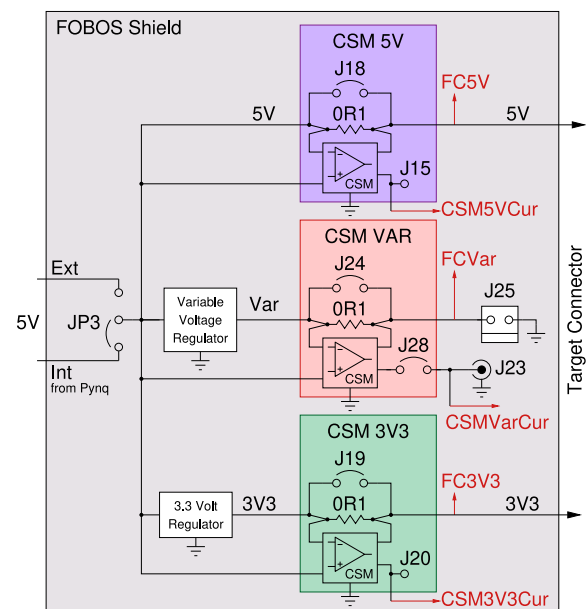


Fig. 6 FOBOS test vector example in hexadecimal notation

whether it is implemented in hardware on an FPGA or in software on a microcontroller.

3.5 Power measurements

The FOBOS Shield has three separate power supply outputs, one 5 V output, one 3.3 V output, and a variable voltage output that can supply between 0.90 V and 3.65 V in 0.05 V steps. The variable voltage output is controlled through the FOBOS Python library and can be configured at any point while the FOBOS Shield is running. This power supply can be used to provide power to the target device such as a Xilinx Artix-7 FPGA which has a core voltage of 1 V. Each of these power sources has a measurement circuit composed of a shunt resistor and an INA225 current shunt monitor (CSM) that can be used to measure the voltage and current. The CSMs have programmable gain that is also configured using the FOBOS

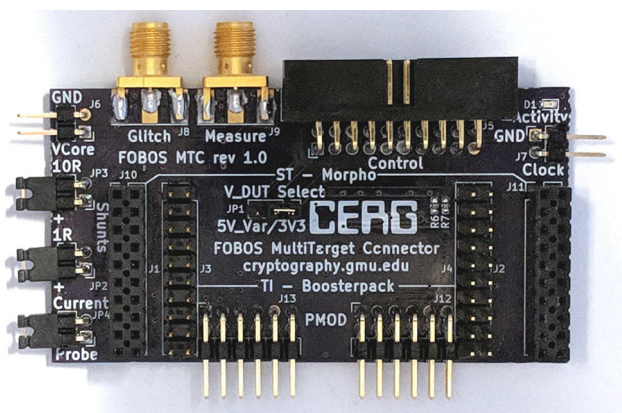


Fig. 7 FOBOS 3 Power Supply and Measurement

Python library. The gain settings in (V/V) are 25, 50, 100, and 200. The error range for these settings are respectively $\pm 0.15\%$, $\pm 0.15\%$, $\pm 0.2\%$, and $\pm 0.3\%$. The diagram of these power sources and their corresponding measurement circuits are shown in Fig. 6.

The average and maximum values are calculated automatically within the FPGA while the target is running and can be read using the FOBOS Python library. There are two methods for sampling measurements from the CSMs. The first is to use the Xilinx XADC, which is an ADC included on the PYNQ board. The XADC has a 12-bit resolution and a 1 MSps sampling rate. Since this single ADC is connected to all current and voltage sources, the effective sampling rate for any single source is 137kHz. Up to 2^{20} samples can be taken before the averaging circuit overflows. Given that a sample is taken approximately every 7.3 microseconds, this corresponds to a maximum measurement time of 7.65 s. The benefit of measurement using the XADC is that it requires no additional hardware and can be easily controlled using software.

The primary drawback of internal measurements using the XADC is the low sample rate. As we will discuss in the case study in Sect. 6.2, this sample rate is acceptable for many applications. However if a higher sample rate is needed, all power outputs may be accessed externally. This allows the user to connect an external oscilloscope with a higher sampling frequency to the signal of interest. The FOBOS software library provides drivers to measure current externally using the SCPI (Standard Commands for Programmable Instruments) interface for programmable oscilloscopes.

3.6 Power calibration

To account for the error tolerances in various components within the power measurement circuitry, a script for calibration is provided. For the variable voltage supply, the voltage

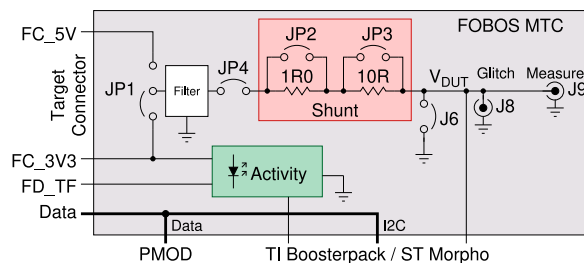


Fig. 8 FOBOS Multi-Target Connector

is calibrated by connecting the variable power source output to a programmable DC Load and comparing the load’s measured voltage against the FOBOS Shield’s measured voltage at various voltages. A polynomial is then fit to the difference between these two measurements and used to correct any error in the measurements. For current calibration of all three voltage supplies, the programmable DC load runs through a series of currents. The same method to calculate an error correction polynomial is used for the current measurement. Since the voltage output of the 5 V and 3.3 V supplies cannot be modified, the voltage measurement is calibrated at the same time as the current. Since a wide range of current draw is used during calibration, the range of variation in voltages is representative of any voltage drop that may occur during normal use.

As an example of the need for calibration of the power measurement circuitry, we discuss the results of calibration of the variable output current measurement. In this example, the current measurement is calibrated for the range [0 mA, 200 mA]. The DC load iterated from 0 mA to 200 mA in 5 mA steps. At each step the actual current consumption of the DC load is recorded as well as the current measured through the FOBOS Shield. With no calibration, on average the FOBOS Shield measure 15% lower than the actual current. With the error correction polynomial calculated from these measurements, the error is reduced to ± 2 mA.

4 FOBOS multi-target connector

We developed the FOBOS Multi-Target Connector (MTC) to easily connect microcontroller boards with the Texas Instruments (TI) LaunchPad or the ST Microelectronics (STM) Morpho connectors as well as FPGA boards with PMOD connectors to FOBOS Control via the FOBOS Target connector (see Fig. 7).

TI Launchpad development kits and STM Nucleo boards are available for a multitude of different processors and instruction set architectures from MSP430 to ARM-Cortex M4. They are cost-effective boards with a built-in programmer and an in-line debugger that connects via USB to a PC. As many of these boards contain only very few components,

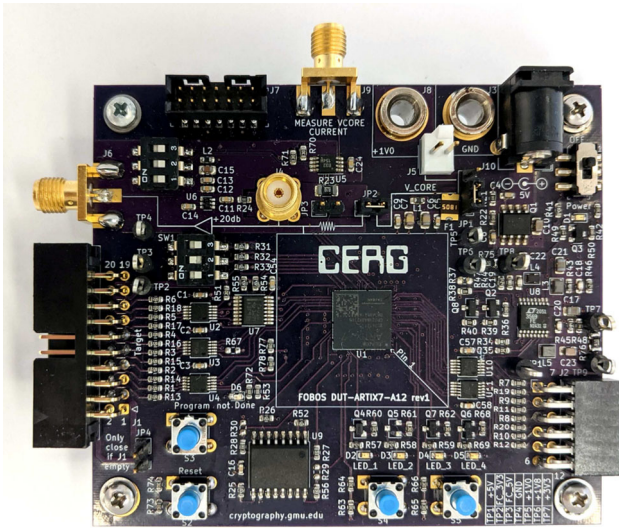


Fig. 9 FOBO MTC Block Diagram

they can be used for power measurement and side-channel analysis. The TI LaunchPad and STM Morpho standard ensure that power, I2C, and general I/O pins are always in the same location. The main drawback of using these boards is, that a clock input is not always provided and might require some soldering, see example in Sect. 6.3. However, this is still much simpler than developing our own target boards with a programmer and a debugger. Data transfer between FOBO Control and microcontroller boards is done via the Inter Integrated Circuit bus (I2C) because of its synchronous nature, speed, and simplicity.

FPGA boards, such as the Nexys and Basys FPGA board series from Digilent Inc., have PMOD connectors. Data transfer between FOBO Control and FPGA boards is done using a 4-bit parallel half-duplex FIFO style protocol, the same that we use for the FBD-A7 and the CW305 DUTs.

Figure 8 shows a block diagram of the MTC. The user can select to use either 5 V or 3.3 V provided by the FOBO Shield to power the microcontroller DUT. An L-C low-pass filter is used to remove noise from the power supply. One of two shunt resistors, 1 Ω or 10 Ω can be selected dependent on the power consumption of the microcontroller. The “activity” LED is powered directly from the 3.3 V supply before the shunt, as not to influence the measurement. Not shown in the block diagram are the pull-up resistors for I2C and the ESD protection for all data and clock lines. The 3.3 V pins on the PMOD connectors are not connected to the power supply. Any attached FPGA board has to have its own power supply. The core voltage of the FPGA can be provided by the variable power supply of the FOBO Shield.

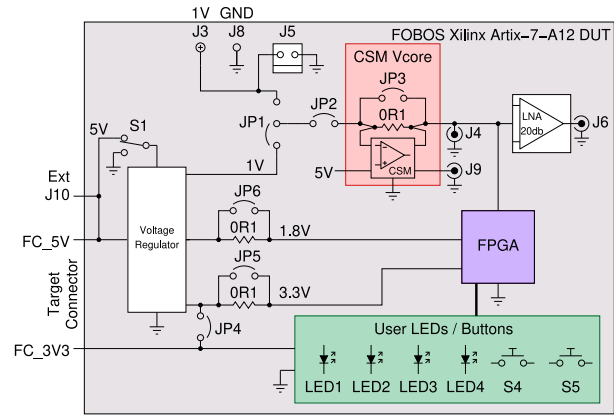


Fig. 10 FOBO Xilinx Artix-7-A12 DUT

5 FOBO FPGA-based DUT

For our DUT we selected the XC7A12T-1CPG238C FPGA from the Artix-7 FPGA family due to its value-based positioning in the marketplace, with the A12T member of the family offering the least amount of programmable fabric making it a likely processing element for a resource-constrained IoT system. This FOBO Xilinx ARTIX7-A12 DUT (or FBD-A7 for short) is shown in Fig. 9.

5.1 Hardware overview

The FBD-A7 enables direct low-noise sampling of V_{Core} current and voltage over SMA connectors. It also provides a low impedance interface to V_{Core} for voltage glitching. The 20-pin target connector is used to receive power and communication signals from the FOBO Shield. Details of the target connector signal allocation are listed in Table 1. The target connector pin-out is compatible with the ChipWhisperer platform. A DIP switch allows for setting of the boot mode to enter the various programming modes. The board features a SPI Flash which can be used to store the configuration bit-stream in non-volatile memory. A header provides access to the JTAG programming interface. The board features user buttons, LEDs, and a PMOD connector. The general system architecture and power distribution are illustrated in Fig. 10. The power subsystem is designed to be powered in three configurations, FOBO Shield powered, FOBO Shield + external supply for V_{Core} , or external supply only. The benchmarking work presented in this paper was performed using the FOBO Shield as the primary power source. Each FPGA voltage rail has connection points that enable direct measurements.

FPGA Programming The FBD-A7 board supports three different configuration modes - Slave Serial, Master SPI, and JTAG configuration mode. The primary configuration mode is Slave Serial mode, as this allows the FOBO 3 Controller

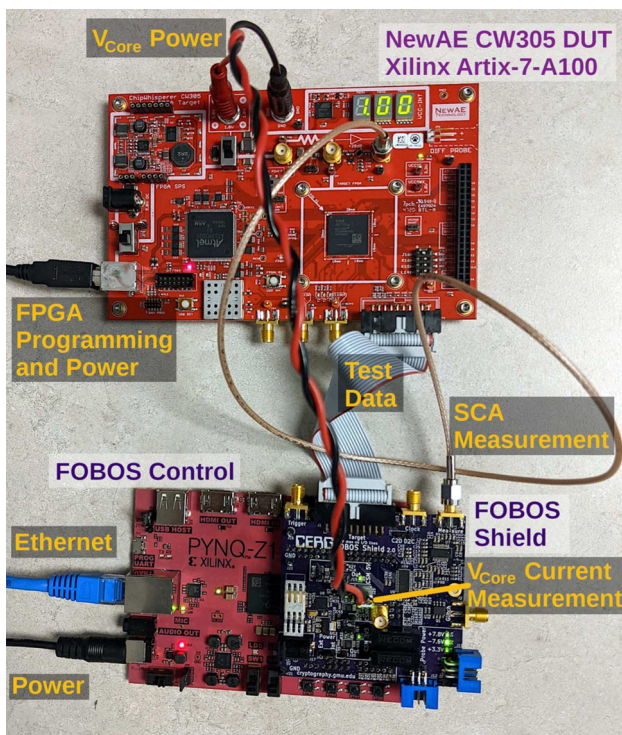


Fig. 11 FBD-A7 Power Measurement

to program the FPGA with a bitstream via the target connector as part of a side-channel evaluation application. In Slave Serial mode, the FC-PROG signal is driven high to enable the alternate boot functions `clk`, `din`, `program-b`, and `init-b`. Due to a lack of conductors on the target connector, four signals were multiplexed using a 4:1 SPDT analog switch. An analog switch was used in lieu of a digital multiplexer due to the bidirectional nature of the digital I/O half-duplex DUT signals. The second FPGA programming method builds on the first method by initially programming the FPGA with a flash interface core and subsequently passing the bitstream through to on-board flash. The advantage of the onboard flash is that the device can self-re-program if it is reset or the power is removed. The third FPGA programming method is JTAG programming via a commercial USB JTAG programmer. The onboard SPI Flash IS25LP256D-JMLE is capable of storing 256MB and was selected from Xilinx's compatible memory list. Since this memory is approved by Xilinx, it can be programmed via Vivado over the JTAG interface. Programming methods 1 and 2 have the added benefit of reducing the overall cost of the FOBOS workstation by not requiring the purchase of a USB JTAG programmer.

Power Consumption: A secondary purpose of the DUT board is to enable measurement of the V_{Core} current consumption. The board contains the same INA225 current shunt amplifier as used on the FOBOS Shield, re-using the 0.1 Ω shunt used for power analysis measurements. The current

shunt amplifier provides 25-200 V/V gain, although bandwidth is limited to 250 kHz, which limits its ability to detect side-channel leakage. The data provided by this measurement interface will be used to quantify the current consumed by the different LWC candidate algorithms

Power Glitching: The board provides access to V_{Core} Voltage via SMA connector for power glitching. Additionally, all signals on the target connector have ESD protection. Voltage glitching involves momentarily shunting the V_{Core} rail to the ground using a PowerFET or other low-impedance switching mechanism. Voltage glitching can result in corrupted register states, erratic state machine behavior, and other out-of-bound type errors.

Design for Cost: The cost was a primary consideration and challenge when designing FBD-A7. The Printed Circuit Board (PCB) layout has four layers, which keeps PCB fabrication costs reasonable. The selected XC7A12T FPGA is the lowest-cost Artix-7 variant offered that still has enough logic resources to implement protected LWC candidates. The total Bill of Material cost for FBD-A7 is \$150, and PCB costs are \$40 bringing the total cost to less than \$200 at the time of this publication.

5.2 Design for side-channel analysis

The primary purpose of the FBD-A7 board is to enable measurement of the V_{Core} voltage rail while the Artix-7 FPGA is performing cryptographic operations. The voltage fluctuations observed on the power rail are so minuscule that preliminary analysis would not detect any leaked information. In order to amplify the side-channel leakage, a BGA 2801 wide-band amplifier is used to provide 22.2 dB of gain. In order to improve the side-channel measurement Signal to Noise Ratio (SNR) performance, various methods are implemented at the PCB level to reduce noise on the V_{Core} voltage rail such as routing critical measurement traces as coplanar waveguides, providing low loss measurement connections, and amplifying the signal in near proximity to the measurement point. V_{Core} can be generated using an integrated switching power supply, whose output is filtered using a low-pass filter. Alternatively, an external power supply can also be used to power V_{Core} . Footprints for V_{Core} voltage rail bypass and decoupling capacitors are present, although component sites are not populated as the capacitors will filter side-channel leakage.

5.3 Side-channel measurement performance

Several FPGA side-channel target boards are available on the commercial market place such as the SAKURA-X and ChipWhisperer CW305. The latter presents a suitable reference point to compare the performance of FBD-A7 since both boards feature Artix-7 FPGA devices and are compatible

Table 2 SNR Measurement Results

DUT	FPGA	SNR(dB)
CW305	XC7A100T-2FTG256	1.816
FBD-A7	XC7A12T-1CPG238C	7.774

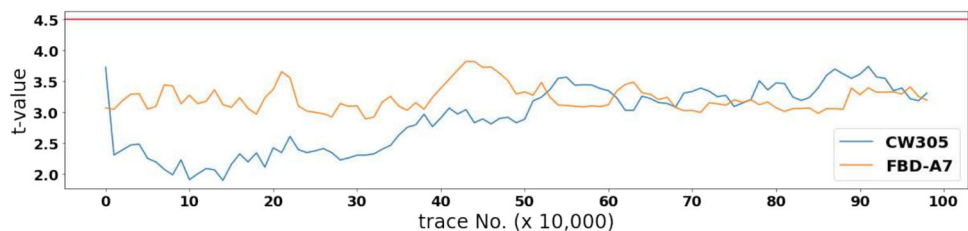
with FOBOS 3 (Fig. 11). The CW305 uses an XC7A100T-2FTG256L FPGA while the FBD-A7 DUT uses the smaller XC7A12T-1CPG238C FPGA. In order to validate the side-channel measurement performance of our design we utilize experimental methods. All performance evaluations are performed without decoupling capacitors on the core voltage rail.

Method 1: SNR Measurement of Side-Channel traces

To validate the performance of FBD-A7 side-channel traces we leverage the method for measuring the SNR performance of side-channel traces set forth by Iokibe et al. [11]. The signal in the context of a side-channel measurement is quantified by calculating the variance of side-channel traces while processing a random data set. Conversely, the noise can be quantified by calculating the variance of side-channel traces while processing a fixed data set. The cryptographic core used for this evaluation is the first-order protected Ascon developed by Amir Moradi's group at Ruhr University Bochum and available at [27]. The CW305 serves as a performance benchmark since it also utilizes an Artix-7 FPGA, the larger XC7A100T-2FTG256. The SNR measurement results are shown in Table 2.

Method 2: Welch's T-Test Comparison Welch's T-test determines if there is any correlation between the observed power traces and the processed data. The benchmark for performance is the CW305 board. The cryptographic core used for this evaluation is the same as used for Method 1. It was built using default Vivado settings. The front-end gain settings were adjusted until the signal exceeded the ADC range, and then reduced to provide some safety margin. The acquisition settings were set the same for both boards. The results of this experiment are displayed in Fig. 12. For both target boards, the result is that after 1 M traces, neither can detect a strong correlation between the processed data and collected power traces. Both target boards trend toward similar values over 1 M traces.

Fig. 12 T-test measurements for LWC Candidate Ascon



Method 3: Measurements to Disclosure Tests

In this test series, we run Correlation Power Analysis (CPA) attacks against a simple, unprotected implementation of the Advanced Encryption Standard (AES). We implemented this 11-clock cycle per round AES with the FOBOS wrapper using Vivado with either the port mapping file (XDC) for the CW305 or the FBD-A7 board. Both implementations require 1328 LUTs, 923 Flip-Flops, and 6 Block RAMs. The control board for these tests is our FOBOS 3 and the measurements were made by the FOBOS Shield. After performing all tests on the FBD-A7 board, the CW305 board was connected to the same FOBOS Shield using the same SMA and ribbon cables to ensure that the setup, cable quality, and location does not influence the comparison. We determine how many encryptions we have to measure the changes in power consumption in order to be certain that we recovered the correct key, known as Measurements To Disclosure (MTD). We perform this MTD test for each byte of the AES key and repeat this test for 10 different random keys. A lot of factors such as the particular layout of the circuit, the value of the key byte, environmental noise, power supply noise, noise from other components on the DUT board, etc. influence how clean the measurement of changes in the current consumption is, i.e., how well they relate to the data being processed. Consequently, we see large variations in the results.

Figure 13 shows the Box and Whiskers plot generated from the MTDs when performing CPA on both boards. The box starts at the 1st quartile till the 3rd quartile showing the median with the center line. The whiskers show the minimum and maximum MTDs. While the maximum is important for breaking all bytes of the key, the graphs are an indicator of the noise in the measurement. The smaller the box and the shorter the whiskers, the less the noise. The first two plots in Fig. 13 compare the FBD-A7 board with the CW305. Recovering all bytes of the keys requires less than 25,000 encryptions on the FBD-A7 board while some key bytes on the CW305 board need almost 4 times as many encryptions. Even the difference between the medians is almost a factor 4. While the CW305 board contains a much larger FPGA than the FBD-A7, the AES implementations require the same amount of resources on the FPGAs of both boards. We think it is unlikely that the larger amount of unused FPGA resources is the reason for the larger noise. However, the larger internal

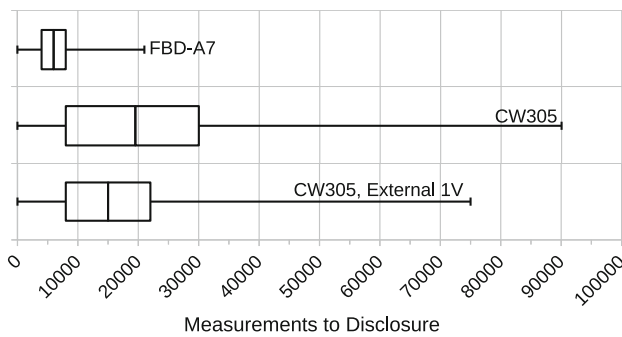


Fig. 13 Comparison of MTD for different boards when performing CPA on an unprotected AES for all key bytes of 10 different random keys

capacitances of the larger FPGA should remove noise. One possible source of noise is the power supply of the CW305. When checking it for noise with an oscilloscope, we could find none. However, powering the core voltage (1 V) of the CW305 from an external lab power supply and repeating all tests we noticed that the MTD results improved as shown in the last plot in Fig 13. The maximum MTD is now less than 4 times that of the FBD-A7 and the median is now less than 3 times larger. Supplying the core voltage from an external power supply also improves the performance on the FBD-A7 board but by less than 7%.

The results of all three methods let us conclude that the side-channel measurement performance of FBD-A7 is similar to or better than that of the CW305.

6 Case studies

6.1 Side-channel protection evaluation of LWC candidate Xoodyak

The effect of synchronizing the sampling and the target clocks on the number of traces needed for key recovery has been observed and discussed in the literature [21]. In this section, we show that performing sampling for leakage assessment using a synchronized clock is significantly more effective in leakage detection. In other words, using synchronized sampling and target clocks, one can detect leakage using significantly fewer traces than setups not using synchronized clocks.

In the following tests, we use a masked implementation of the NIST LWC finalist Xoodyak. This implementation is based on an unprotected design by the Xoodyak Team [30] and protected by Amir Moradi's group at Ruhr University Bochum with the help of the AGEMA tool [14]. While AGEMA is able to add protection to the datapath of the design, the control logic has to be manually modified. Our TVLA tests show leakage which was identified as an issue

with providing random bits at some clock cycles. This was a bug in the control logic. It since has been fixed.

We performed TVLA tests on the masked implementation of Xoodyak using an external oscilloscope at a sampling rate of (test A) 1 GS/s with 8-bit resolution and (test B) 125 MS/s with 15-bit resolution. We repeated the same experiment, but this time, we used FOBOS 3 to capture traces at 50 MS/s with 10-bit resolution (test C). In the FOBOS 3 case, the ADC clock is synchronized with the target clock, while the external oscilloscope sampling clock is not. Table 3 shows the details of each experiment and the corresponding results. In all cases, we used the exact same Xoodyak implementation, which was instantiated in the NewAE C305 and ran at 10 MHz, and we used the same fixed-vs-random test vectors. Figure 14 shows the maximum t value in each experiment as a function of the number of traces processed. The red line marks the 4.5 thresholds with t values exceeding this threshold, indicating leakage detection. The figure shows that in test C, which uses the synchronous clock, the t values exceed the threshold after processing 1.3 million traces. For experiment A, which uses a much higher sample rate but less resolution, the test detects leakage after processing 1.6 million traces, while in experiment B which uses a higher sample rate **and** much higher resolution, the leakage is detected after 8.7 million traces are processed.

Test results from other teams for the above masked Xoodyak implementation and publicly available at [5] are listed as tests D and E in Table 3. No leakage was detected after processing 10 million traces in the two cases. In both tests, the clock and target clock are not synchronized. In the case of test D, the sampling rate is lower than in all of our experiments. The lack of clock synchronization combined with the lower sampling rate and resolution differentiates this test from test C. For test E, however, the sampling rate is similar to test A, but the hardware target used is different, so the comparison is not straightforward.

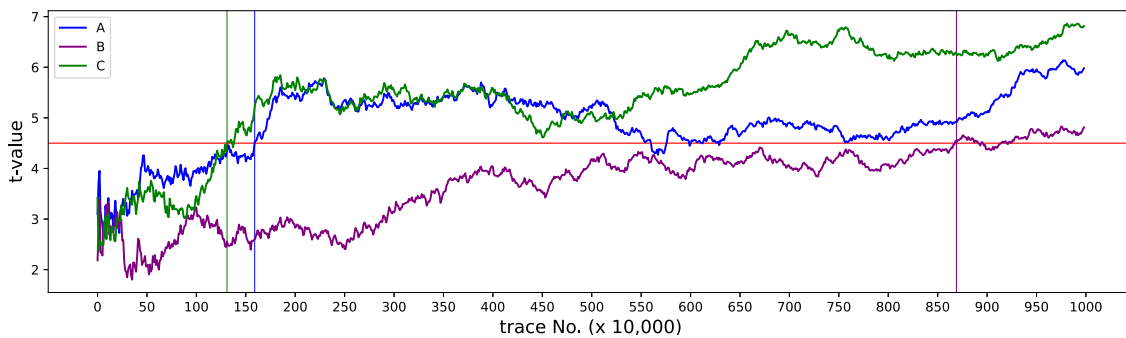
These results show that TVLA results should be taken cautiously since test parameters, particularly clock synchronization, significantly affect the test results. Additionally, using synchronized clocks can save the evaluation lab's time since leakage is detected using fewer traces. At the same time, a lower sampling rate can be used, which translates to cheaper equipment.

6.2 Power and energy consumption of LWC candidate Ascon

To show the power measurement capabilities of FOBOS, we provide a case study showing the power consumption results for the hardware reference implementation of the LWC winner Ascon [24]. We performed power measurements for two different variants of this design - one lightweight design and one high-performance design. The lightweight

Table 3 TVLA results of masked Xoodyak implementation based on measurement setup, all ran for 10 Million traces

Lab	Scope	DUT	Resolution	Sync.	Sample rate	DUT freq.	Fails at traces	Test
Ours	PicoScope 5244D	CW305	8 bit	No	1 GS/s	10 MHz	1.6 M	A
	PicoScope 5244D	CW305	15 bit	No	125 MS/s	10 MHz	8.7 M	B
	FOBOS 3	CW305	10 bit	Yes	50 MS/s	10 MHz	1.3 M	C
TU Graz [29]	PicoScope 6404C	CW305	8 bit	No	22 MS/s	1 MHz	Pass	D
Tsinghua [32]	LeCroy Wave Runner 8404M	SAKURA -X	8 bit	No	1 GS/s	6 MHz	Pass	E

**Fig. 14** Maximum t-value vs. the number of processed traces. Vertical lines indicate the point at which the t-value exceeds the threshold in each test

implementation, designated v1, requires 1,465 LUTs, has a maximum frequency of 191 MHz, and has a throughput of 1.53 MB/s. The high-performance implementation, designated v5, requires 2,797 LUTs, has a maximum frequency of 150 MHz, and has a throughput of 2.4 MB/s. This experiment was performed using a CW305 target board as well as the FBD-A7 board discussed previously. Power measurements were taken using both the XADC on the PYNQ board and an external oscilloscope with a sampling rate of 4 GSa/s and a resolution of 8 bits. Long messages with 8 KB of plaintext and 8 KB of associated data were taken to limit the impact of the transition period for the current consumption at the edges of the measurement. For the CW305 board, the power to the FPGA core is provided using the variable voltage output on the FOBOS Shield, which allows the current and voltage to be measured on the FOBOS shield. For the FBD-A7 board, the current consumption for the FPGA core can be measured using the measurement circuit on the DUT board.

First, we will discuss the comparison of results from the measurements taken using the XADC versus the external oscilloscope. Traces of the current and voltage were taken while the DUT was running at the following frequencies: 5 MHz, 25 MHz, and 50 MHz. The average current values from both the Shield and oscilloscope are shown in Table 4. The average power is calculated by taking the average current consumption and multiplying by the average voltage. Energy is determined using the calculated average power and latency, as well as using the area under the curve for the oscilloscope trace. An example trace from the external oscil-

loscope is shown in Fig. 16. The light shaded area represents the static energy, and the dark area represents the dynamic energy. In the trace-aligned measurements, the power is calculated from the start of the trigger until the power returns to the static power level. The FOBOS measurements only support trigger-aligned measurements, and thus do not account for the discharge energy after the operation completes.

As expected, we note that the energy calculations using average power and area under the curve are nearly identical. We can also observe that there is a small, but noticeable, difference between the trace-aligned and trigger-aligned measurements. The difference in energy consumption varies between $0.01 \mu J$ to $0.9 \mu J$. However, this represents a difference of less than 0.05% in the worst case. Even with the lower sample rate of the XADC, the average current is close to that of the external oscilloscope. As observed in Fig. 15, the current consumption is smoothed out by the capacitance of the target device. Thus there are no instantaneous spikes in power consumption, which allows the lower sampling frequency of the FOBOS Shield to achieve similar accuracy to the oscilloscope with a much higher sampling rate. The FOBOS measurements are within 5% of the oscilloscope for all frequencies. However, we can observe that the number of samples for the 50 MHz design is already low. Thus for hardware with very low latency, the Shield will not gather enough measurements to produce a meaningful result.

Next, we will discuss the comparison of results between the CW305 and FBD-A7 DUT board. Since the FPGAs on these boards vary substantially in their size and speed

Table 4 Average Current Measurements of Ascon-v1 Encryption 8KB of AD and 8 KB of PT Using XADC and Oscilloscope

Frequency	Oscilloscope				Area under curve					
	FOBOS (XADC)	Trace average	Trace-aligned	Trace-aligned	Power (mW)	Energy (μJ)	Num. samples	Power (mW)	Energy (μJ)	Num. samples
50MHz	33.63	109.32	446.6	32.886	106.87	1299933	32.887	106.88	106.87	1312390
25MHz	46.49	30.22	89.4	44.44	28.89	1299936	44.347	28.82	28.82	1350269
5MHz	61.45	19.97	44.8	59.39	19.3	699881	59.1	19.21	19.21	649971

grade, we do not expect similar power consumption from both devices. The traces for the 8KB PT, and AD on both target boards are shown in Fig. 15. For power and energy results, we compare measurements taken using the external oscilloscope. We also generated power estimates using the power estimation feature of Vivado with the inclusion of the post-implementation timing simulation signal activity.

Table 5 and Fig. 17 show the power and energy results for each of the target boards. The relationship between power and frequency can be represented as a linear equation $p = a + b \cdot freq$ where a is the static power and $b \cdot freq$ is the dynamic power. For these two designs and platforms, the power is represented by the following equations:

$$\begin{aligned}
 p_{cw305_v1} &= 0.39 \cdot freq + 28.25 \text{ mW} \\
 p_{cw305_v5} &= 1.33 \cdot freq + 26.4 \text{ mW} \\
 p_{fbd-a7_v1} &= 0.38 \cdot freq + 9.22 \text{ mW} \\
 p_{fbd-a7_v5} &= 1.28 \cdot freq + 9.1 \text{ mW}
 \end{aligned}$$

As expected, the smaller component has substantially lower power consumption. This difference is primarily due to the lower static power, which is only approximately 9 mW and 27 mW for the FBD-A7 and CW305 respectively. The dynamic power of both boards varies very little, which is expected since the number of state transitions is independent of the target device and both devices are in the same family of FPGA. We can also observe slight differences in the trace of the voltage across the CSM shown in Fig. 15. While there are no capacitors in the V_{core} power circuitry of either board, the chip does have some internal capacitance. We can see that the CSM trace of the smaller chip used in the FBD-A7 board is less affected by this internal capacitance. We can also represent the estimated power as a function of the clock frequency as shown below. When comparing the estimated results to the experimentally measured results, we can see the limitations of this power estimation tool. First, the static power is significantly higher than what was observed in our measurements and even shows the smaller device having higher static power consumption. We can also observe that the dynamic power estimate accuracy decreases with design complexity. The dynamic power for the smaller design is close to the experimental results, but for the larger design, it is substantially higher.

$$\begin{aligned}
 p_{cw305_v1_est} &= 0.33 \cdot freq + 60.6 \text{ mW} \\
 p_{cw305_v5_est} &= 2.71 \cdot freq + 81.44 \text{ mW} \\
 p_{fbd-a7_v1_est} &= 0.36 \cdot freq + 85.41 \text{ mW} \\
 p_{fbd-a7_v5_est} &= 2.34 \cdot freq + 111.26 \text{ mW}
 \end{aligned}$$

These results align with the findings of several previous works comparing estimates and measurements for older versions of Xilinx's and Intel's power estimation tools. One previous work had performed similar experiments with common cryptographic implementations such as AES and DES and found the error of the estimate varied between 17% and

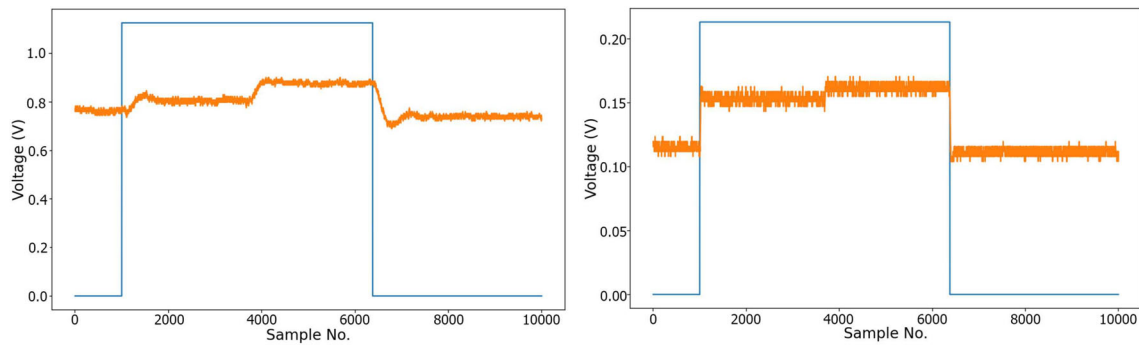


Fig. 15 CSM voltage during Ascon-v1 encryption of 8 KB of AD and 8 KB of PT at 45 Mhz. Left: CW305. Right: FBD-A7

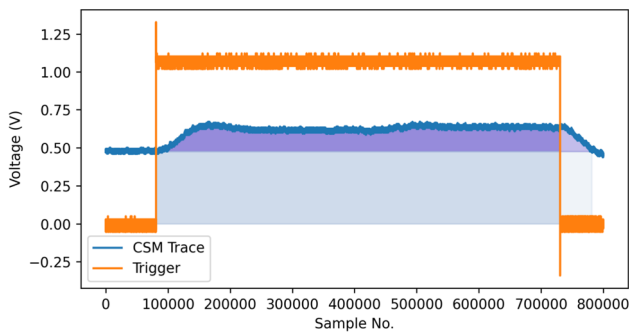


Fig. 16 Example Power Trace

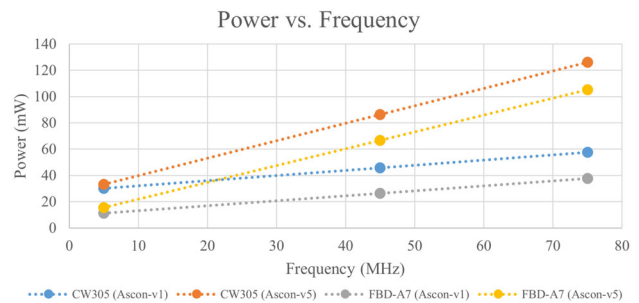


Fig. 17 Comparison of Power Consumption at Different Frequencies for CW305 and FBD-A7

200% [17]. Another work compared estimates and measurements for Spartan-6 FPGAs in which they compared results for several different types of algorithms, including AES, a Fast Fourier Transform, and multiple different implementations of a 32×32 -bit multiplier. The estimation’s error varied between -5% and 377% depending on the design and implementation language [22]. A similar work that compared estimates and measurements for various implementations of a 32×32 bit multiplier on a Cyclone-III FPGA

found that the estimates were much more accurate, varying between -11.7% and 13% error [23]. These results show the importance of real-world measurements when analyzing the efficiency of hardware running on FPGAs.

6.3 Differential power analysis of AES on MSP430

In this case study we show how we used FOBOS to attack an implementation of AES on a TI-MSP430 microcontroller.

Table 5 Power and Energy Results for FOBOS Artix-7 DUT and CW305 Targets

Target	Design	Frequency	Power (mW)		Energy (μ J)		Latency (ms)
			Measured	Estimated	Measured	Estimated	
CW305	Ascon-v1	5	29.99	62	97.46	201.44	3249
	Ascon-v1	45	45.62	76	16.47	27.44	361
	Ascon-v1	75	56.43	85	12.23	18.36	216
	Ascon-v5	5	33.00	93	53.68	151.22	1626
	Ascon-v5	45	86.18	208	15.58	37.44	180
	Ascon-v5	75	125.91	282	13.65	30.46	108
FBD-A7	Ascon-v1	5	11.19	87	36.37	282.66	3249
	Ascon-v1	45	26.23	102	9.47	36.82	361
	Ascon-v1	75	37.89	112	8.18	24.19	216
	Ascon-v5	5	15.65	121	25.46	196.75	1626
	Ascon-v5	45	66.15	221	11.96	39.78	180
	Ascon-v5	75	105.07	284	11.35	30.67	108

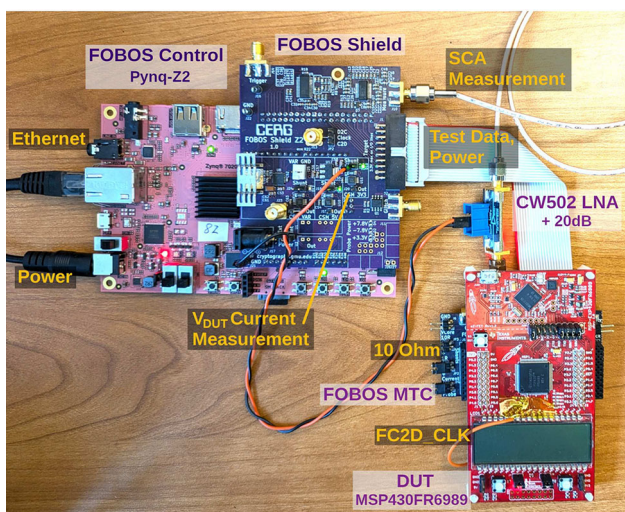


Fig. 18 FOBO3 setup with MTC and TI-MSP430 Launchpad as DUT

Figure 18 gives an overview of the setup. The control board is a Pynq-Z2 board with a FOBO3 Shield attached. Test vectors and power are transferred via ribbon cable to the FOBO3 MTC onto which the MSP430 LaunchPad is mounted. The V_{DUT} selector of the MTC is set to 3.3 V. MSP430 microcontrollers are known for their ultra-low power consumption. The MSP430FR6989, which we are using in this case study, is based on low-power Ferroelectric RAM technology (FRAM for short) and, according to its data sheet, consumes only $100 \mu A$ per MHz. In this experiment, we provide a 1 MHz clock to the microcontroller. In order to obtain a sufficiently large signal, we chose the 10Ω shunt resistor of the MTC and attached the CW502 low noise amplifier from NewAE to boost that signal by 20 dB. As the probe power supply option is not populated on this FOBO3 Shield, we powered the amplifier from the 3.3 V power supply on the FOBO3 Shield. The LNA of the FOBO3 Shield is set to its largest gain of 55 dB. With these settings we obtain the power trace shown in Fig. 19 which is near full scale ($0 \dots 1023$) of the ADC.

Synchronized measurements can be achieved by providing the clock signal for the MSP430 by the FOBO3 Control board. While the FC2D_CLK signal is available on the PMOD connector of the MTC, the corresponding pin on

Fig. 19 2,000 samples of 12,000 collected during first round of AES on MSP430 running at 1 MHz, sampled at 4 MSps

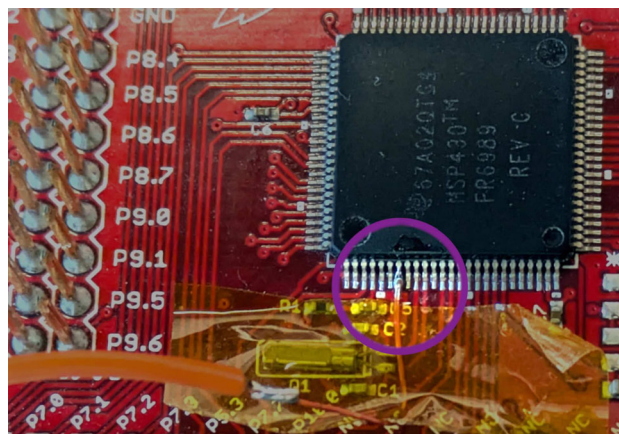
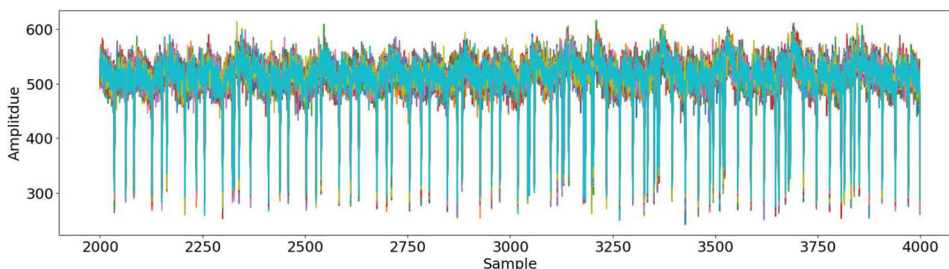


Fig. 20 MSP430FR6989 connection of external clock

the MSP430FR6989 chip is not available on the LaunchPad headers. Therefore, this LaunchPad board required a small modification; we soldered a wire directly to the external clock pin of the MSP430 as shown in Fig. 20 and connected it to FC2D_CLK.

We programmed the microcontroller with the publicly available AES implementation from [16] along with a wrapper that handles communication with the control board using I2C. The AES implementation runs first a key expansion and then the actual encryption. This implementation requires 30,000 clock cycles for the AES encryption after the key expansion. We sample at 4 Mega Samples per second (MSps), i.e., 4 samples per clock cycle. We then collected 16,000 traces of 12,000 samples each, for the first round of AES encryption using a fixed key and random plaintext.

We performed a correlation power analysis (CPA) attack [4] on the first-round S-box output. We used hamming weight (HW) as a power model since it is a suitable model for software implementations' power consumption. CPA attacks require an intermediate value that is calculated as a function of known data and a small part of the sensitive information (e.g. key) called a subkey. The attacker guesses the subkey and calculates the intermediate value which is used to estimate the power consumption using the power model. The estimated power of several cryptographic operations is then correlated with the actual power consumption and the guess with the highest correlation is picked. This process is repeated

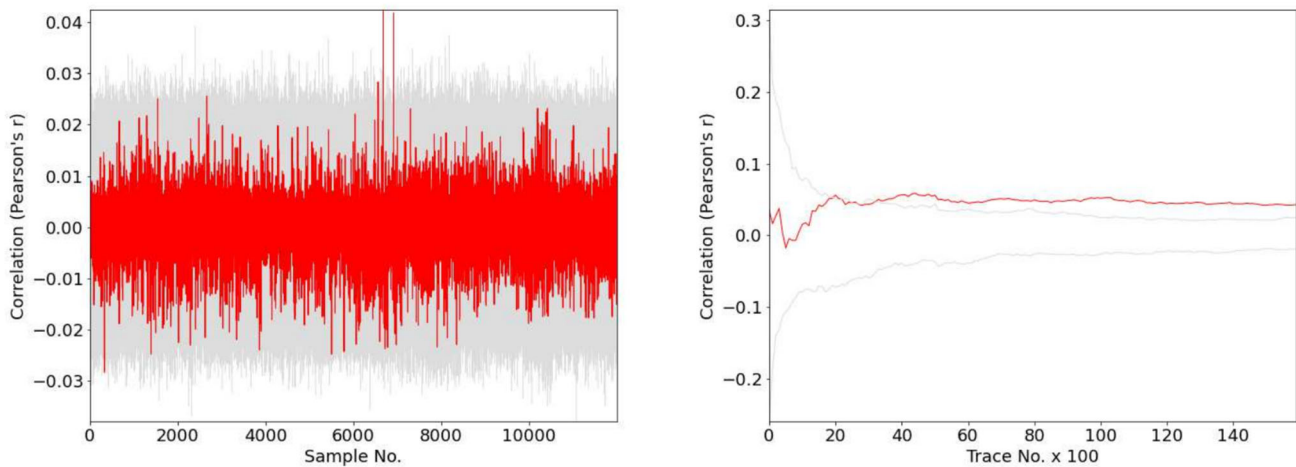


Fig. 21 CPA results for the correct guess of the first byte of the key (red) compared to wrong guesses (gray). Left: Correlation graph. Right: MTD graph

until all subkeys are revealed. In our attack, the power model used is $HW(Sbox(k \oplus pt))$ which is the hamming weight of the S-box output in the first round. Here, k and pt are one byte of the key and input plaintext, respectively. We used the FOBOS analysis module which receives the power traces and the plaintext, calculates the estimated power using the specified power model, and runs CPA. Figure 21 shows the correlation and the MTD graphs for the first byte of the key which was correctly revealed. From the MTD graph, we can see that less than 4,000 traces were sufficient to distinguish the correct key guess of this subkey. Overall, we were able to recover 6 subkeys and 4 more subkeys are amongst the top candidates that were found. The remaining 6 subkeys require more than 16,000 traces using this setup and our CPA attack using the simple hamming weight power model. More advanced techniques as described in [18] might require fewer traces. Nevertheless, this test confirms the capability of our setup to mount power analysis on software targets even on ultra-low power microcontrollers.

7 Conclusions

This paper presents an open-source, multi-user platform for side-channel analysis and benchmarking. We introduced the FOBOS Shield which in conjunction with a PYNQ-Z1 or a PYNQ-Z2 form the FOBOS Control board which is capable of synchronized SCA measurement as well as power and energy consumption measurements. Additionally, we introduce a new low-cost FPGA target board and evaluate its performance. Furthermore, we introduce a Multi-Target Connector which allows for connecting TI Launchpads and STM Nucleo boards to FOBOS for performing SCA measurements of microcontrollers. Our three

case studies highlight the features of FOBOS 3 and its application to the evaluation and benchmarking of hardware implementations of the finalists in the NIST LWC standardization process, and evaluating cryptographic implementations on microcontrollers. All files required for building and running FOBOS 3 are provided under Apache 2 License (allowing commercial usage, requiring attribution) at <https://github.com/GMUCERG/fobos>. This includes HDL files (not including Xilinx IP) and Python for control, schematics, and board design files for FOBOS Shields, FBD-A7, FOBOS-MTC, etc. Future work on this platform will be the support of the NewAE CW308 UFO board for targeting more microcontrollers and the development of target boards for other popular FPGA families.

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Author Contributions All authors contributed to writing the paper. Eduardo Ferrufino designed the FBD-A7 target board and performed all validations, Luke Beckwith wrote the software for power measurement and performed the case study of power and energy consumption of LWC candidate Ascon, Abubakr Abdulgadir is the original developer of the FOBOS 3 software, Jens-Peter Kaps is the professor supervising the current graduate students Eduardo and Luke, he is also the project lead and developed both FOBOS Shields, the FOBOS MTC and the power measurement circuitry and soldered all boards.

Data availability The datasets generated for this study are not available due to their size. However, FOBOS 3 is available at <https://github.com/GMUCERG/fobos>

Declarations

Conflict of Interest The authors declare no competing interests.

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