ECE 493
Final Report

RF Detector for Shielding Effectiveness Testing (RF DSET)

Abstract:

This system is designed to detect and record the RF shielding effectiveness of a given enclosure. Our system consists of two main devices, the Detector Unit and the Source Monitor Unit. The testing to be completed involves a series of broadcasted RF signal sweeps over 8 hours. This RF sweep occurs in a test environment in order to characterize the enclosure-under-test. These devices are first connected, allowing their clocks to synchronize. Before beginning testing, the Detector Unit is placed inside the enclosure-under-test, attached to a custom RF antenna within the enclosure-under-test, and begins detecting and recording incoming data with timestamps. The Source Monitor remains connected to the computer controlling the RF signal transmission and the RF signal generator sweep sync output. It timestamps the start of each linear frequency sweep. Following the conclusion of the test, the Detector Unit is retrieved, and the two devices are connected. The devices then share their data, synchronizing detected data from the Detector Unit with that of the Source Monitor. This provides the necessary data to compute the shielding effectiveness of that enclosure for the range of frequencies performed in the test.

A quick summary of the requirements: Maximum dimensions 6”x6”x3”, external SMA connector, 8 hours minimum battery life, stores data internally, 100 MHz – 6 GHz frequency range, minimum detectable power of -30 dBm, dynamic range of 30 dB, storage for 6.93 million samples.

Date of Submission: 4/26/2019

Team Members:
Kevin Riley
Shahed Afrad
Steve Kim
David Phelps

Faculty Supervisor: Dr. Jens-Peter Kaps

1. Table of Contents

2. Executive Summary

In this age of high-tech machinery and complex circuitries, the slightest disturbance within a system can have huge impact on the proper functionality. One such disturbance is electromagnetic interference caused by a Radio Frequency (RF) environment. To mitigate and prevent outside influence penetrating an enclosed system, shielding material is provided, and before implementation of the shield, it goes through a vital process of electromagnetic susceptibility testing.

The RF exposure in the environment is unpredictable, and to fully compensate for the wide range of RF, Shielding Effectiveness (SE) testing is one of the options for testing electromagnetic susceptibility. The shield enclosure is placed in a stirred chamber that sweeps typically from 100kHz to 10GHz. The current method for this testing utilizes a strategic placement of antenna inside the enclosure which is physically wired to the outside analysis unit. The process is time-consuming and labor intensive due to the nature of physical alteration of the shield. Also, the process might compromise the accuracy of the testing.

We have developed two devices that will forgo the process of drilling a hole in the shielding for the antenna to be placed and connected. One of our devices is a battery-powered RF detector unit with antenna attached, which will record incoming RF and Microwave signals inside the encloser. The other device is a source monitor unit, which will be synced to the analysis unit to record the RF sweep information. With these two devices, the enclosure does not have to be modified, which is a preferred way for the owners of the enclosure-under-test. Also, time and labor required for the current method, which can take hours of preparation and designing, can be saved. The success of our devices proves the possibility of a noninvasive approach to the testing which can be further developed in the future.

To succeed, we needed a thorough understanding of the current procedure of SE testing and the modifications that we will be making. The circuitry components, especially the ones concerning RF-carrying and processing modules, as well as printed circuit board, PCB, design were researched extensively, and since our devices have multiple components and stages, thorough testing of steps was implemented to acquire the optimal accuracy of the recording. Furthermore, power management was an important factor since battery must run for about a span of eight hours, and we have developed robust and optimized devices.

3. Approach

3.1 Project Origin

One of our team members is employed by our customer, NSWC Dahlgren Electromagnetic Environmental Effects Assessment and Evaluation Branch, B52. As discussed in the executive summary, our customer runs test on the shielding effectiveness of various types of enclosures. The enclosure-under-test is placed inside a special chamber, or room, for testing. This room is capable of radiating a wide range of RF and Microwave frequency signals into the chamber to test the shielding effectiveness of the enclosure in this frequency range. Their current method of testing involves drilling a hole in the enclosure-under-test, attaching a coaxial cable to the custom antenna inside the enclosure, and running that cable out of the testing environment. The retrieved signals are then used to determine the shielding effectiveness of that enclosure, compared to the known signals that were radiated during the test.

This method was not ideal as the drilling damages the enclosure and could compromise its shielding effectiveness, so the customer asked us to design a less invasive method of testing. Specifically, they wanted a device that could be placed inside an enclosure-under-test that does not require drilling or other such damaging methods. Thus, the RF Detector for Shielding Effectiveness Testing (RF DSET) was born.

3.2 Solution to the Problem

We quickly determined that a detector capable of recording and storing data would need to be placed inside the enclosure-under-test. Since this unit would not know what exactly was being radiated into the test chamber, a second device would be needed to monitor this data. Therefore, we had to create a two-device system that worked together. We named these two devices the Detector Unit and the Source Monitor.

In order to lay the foundation for the project, we discussed and agreed upon the specifications and requirements of the project with the customer. It was determined that we would provide a working prototype of the system, with the understanding that it will prove the concept, and that a more advanced (and expensive) version could be pursued by the customer at a later date.

Once the requirements and specifications were solidified, we continued with a top-down approach to designing the system. The high-level inputs, outputs, and functions of each of the two devices were determined and then broken down further. The Detector Unit needed to receive

the RF signal, amplify it in some cases, logically detect it, quantify it, timestamp it, and record it. The Source Monitor needed to synchronize with the Detector Unit, pull the data from it, and match the retrieved data with the monitor data. Soon we had our system architecture and functional decompositions. This led us to our physical architecture and system architecture.

Once our top-down design had progressed to the point where we were comfortable with the direction of the project, we began work on the circuit diagrams for each device. After discussing and re-drawing these diagrams, we settled on a general circuit design.

With our general circuit design in hand, the exciting part began. We spent a large amount of time researching and choosing the specific components we would need, such as the NLB-300 RF Amplifier or the MSP430 microcontroller. We elected to spend a large amount of time on this process, because in the frequency range we were working in, the component selection was very important. For instance, we had to ensure that the components in our RF signal path worked in our frequency range, and we had to determine whether or not the 50 Ohm impedance matching was done internally or needed to be done externally.

Once we had selected and, in many cases, ordered all active or specialty components, the real work began. Half of the team was dedicated to writing or finding all necessary pieces of software, and the other half was dedicated to PCB design. Looking specifically at PCB design, one of the biggest challenges was ensuring that all RF signal traces were impedance matched to 50 Ohms. This involved heavy research into methods like striplining, microstripping, and coplanar waveguides. Simultaneously, the actual footprint selection or footprint design for components was underway, followed by board layout. After trying out different methods for impedance matching, and designing then redesigning the PCB, the grounded coplanar waveguide method was decided upon. This occurred after settling on a board fabricator and reviewing the datasheet for the material used in their four-layer boards. The grounded coplanar waveguide method yielded a very consistent characteristic impedance in the 100 MHz to 6 GHz frequency range while allowing for trace dimensions that worked well with our components and the fabricator.

Having finished the PCB design for the Detector Unit, the remaining components were ordered, and the board was sent out for fabrication. All components arrived in two weeks, and the soldering process began the following week. The Source Monitor is a different story. Due to the nature of the Source Monitor, the customer agreed with our assessment that it was not

necessary to design a complete PCB for the Source Monitor, only for the Detector Unit. Instead, the Source Monitor makes use of the MSP430F5529 LaunchPad. While we would have liked to design a PCB for the Source Monitor, we simply did not have enough time.

These two devices, the Source Monitor and Detector Unit, work together to achieve a solution to the initial problem. The Detector Unit can be placed inside the enclosure-under-test for the duration of the test, all the while detecting and storing any RF or Microwave signals that it detects, at either no gain or high gain. That data is timestamped and compared to the data recorded by the Source Monitor. Since the Source Monitor keeps track of exactly what frequencies, and at what power, were radiated at a given time, the data is synchronized to determine the shielding effectiveness of the enclosure, without drilling a single extra hole!

3.3 Contributions

Kevin Riley was essentially the chief engineer for this project, as well as the liaison between the team and the customer. He was in charge of the software portion of the project and was instrumental in the overall design of the system. Kevin was the Project Manager for the first half of the project, until it was evident that the software portion of the project took too an incredible amount focus and time. David Phelps was the lead PCB designer and was in charge of selecting and integrating a power supply. David worked heavily on the administrative side of the project and was the Project Manager for the second half of the project, although the birth of his second child also took away some of that focus. David also selected and acquired the remaining components following PCB design. Steve Kim was also part of the PCB design and assembly team and worked heavily on the administrative side alongside David. Steve also focused greatly on component selection and acquisition. Shahed Afrad was on the software team and was tasked with PCB assembly and did so very quickly and efficiently. Shahed, like Steve, helped greatly with component selection and administrative tasks.

4. Technical Section

4.1 Functional Decomposition of Detector Unit

The main functions of the detector unit are the signal processing, control processing, time synchronization, and power managing with inputs and outputs as shown in *Figure 1*. This unit will be the one placed inside the enclosure with purpose of recording the RF as DC power with timestamp onto the SD card after initiation by time delay. *Figures 2-6* describes the detailed functionalities of each modules with connections of inputs and outputs.

4.1.A Level-0 Top-Level Functions

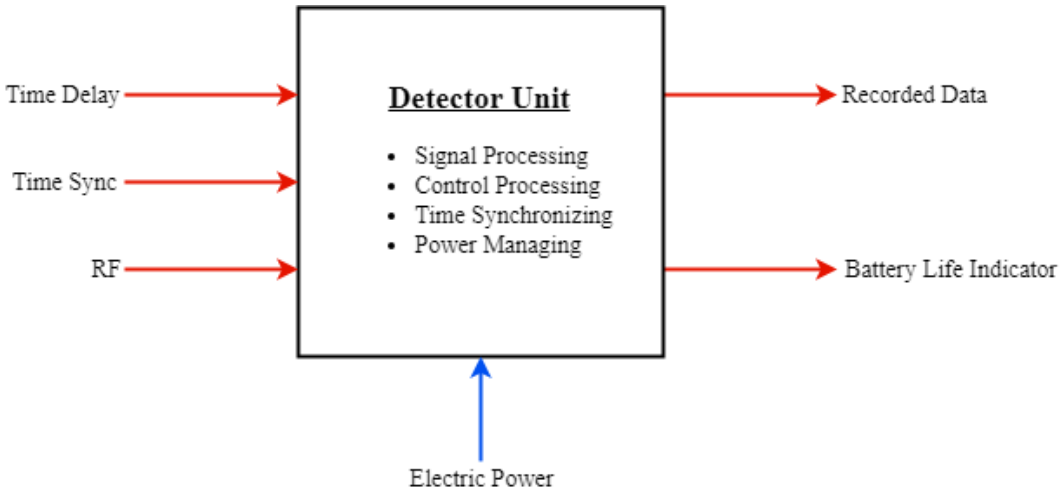


Figure 1: Level-0 Top-Level Functions of Detector Unit

4.1.B Level-1 Functional Decomposition

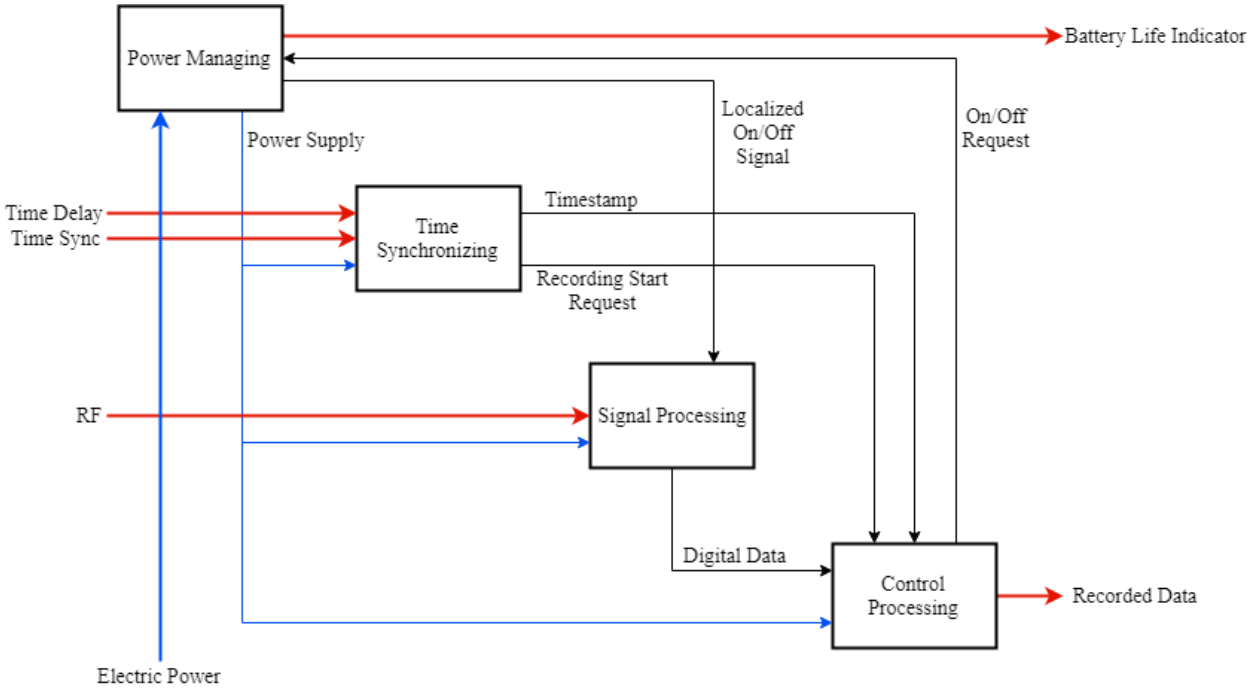


Figure 2: Level-1 Functional Decomposition of Detector Unit

4.1.C Level-2 Functional Decompositions

<u>Function: Power Managing</u>

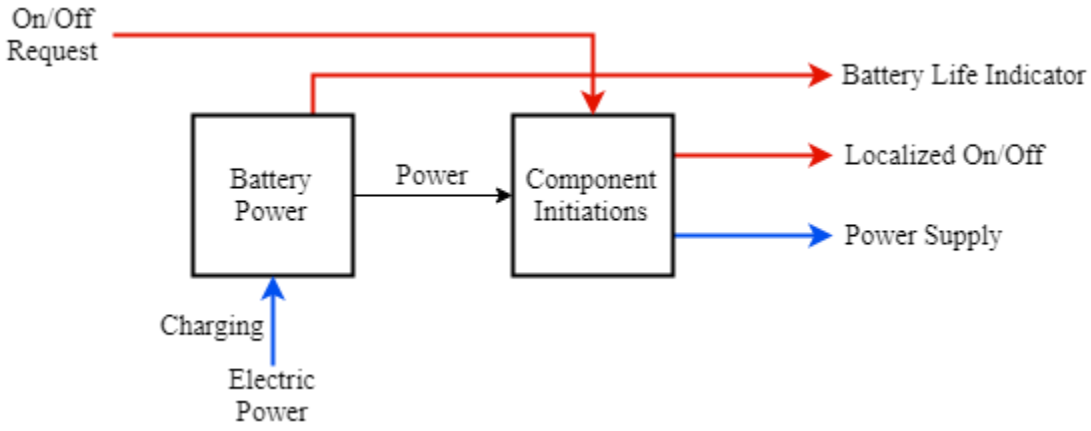


Figure 3: Level-2 Functional Decomposition of Power Managing

Function: Time Synchronizing

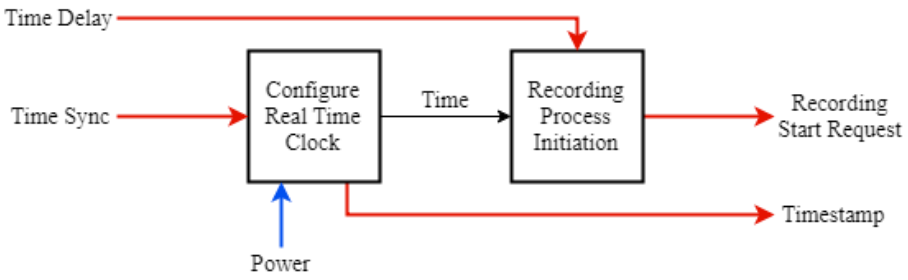


Figure 4: Level-2 Functional Decomposition of Time Synchronizing

Function: Signal Processing

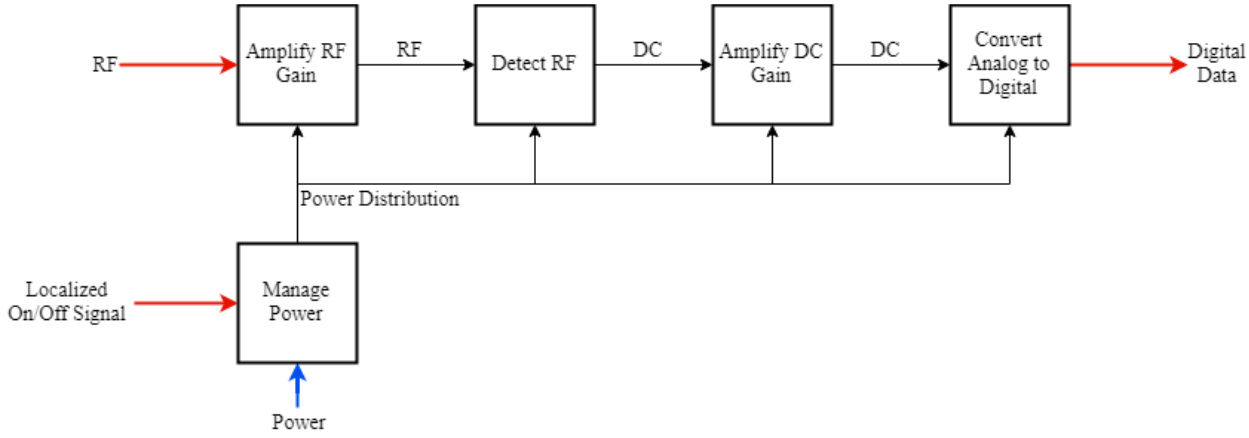


Figure 5: Level-2 Functional Decomposition of Signal Processing

Function: Control Processing

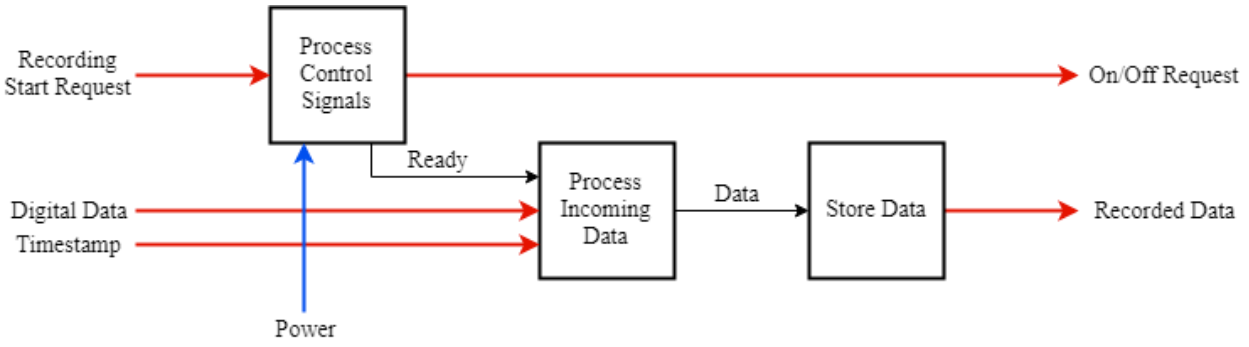


Figure 6: Level-2 Functional Decomposition of Control Processing

4.2 Functional Decomposition of Source Monitor Unit

The main functions of the source monitor unit are time synchronizing, control processing, and displaying relevant information with inputs and outputs as exhibited in *Figure 7*. This unit will be connected to the source computer that runs the RF sweeps and will record necessary information. Another important purpose the source monitor unit serves is when the source monitor unit is connected to the detector unit, in which it acts as the bridge between the source computer and the detector unit for transferring data and power. *Figures 8-11* shows the detailed functionalities of the modules with connections of inputs and outputs.

4.2.A Level-0: Top-Level Functions

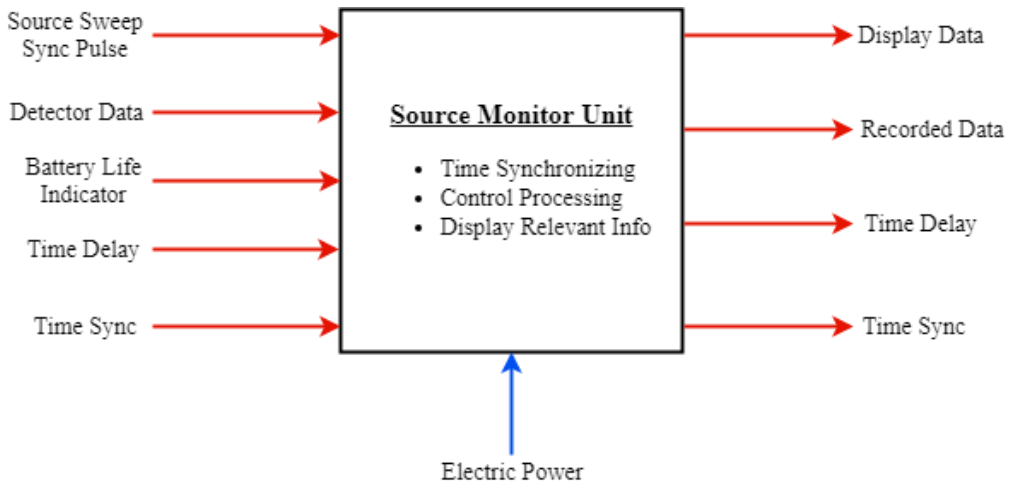


Figure 7: Level-0 Top-Level Functions of Source Monitor Unit

4.2.B Level-1 Functional Decomposition

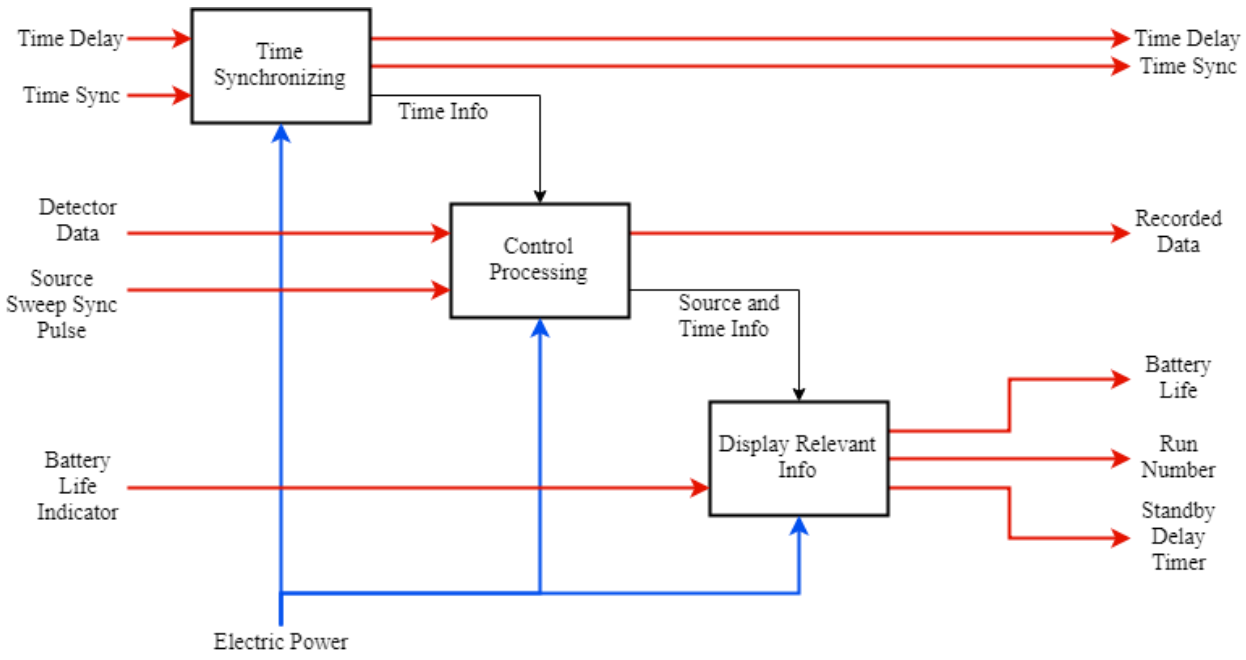


Figure 8: Level-1 Functional Decomposition of Source Monitor Unit

4.2.C Level-2 Functional Decompositions

Function: Time Synchronizing

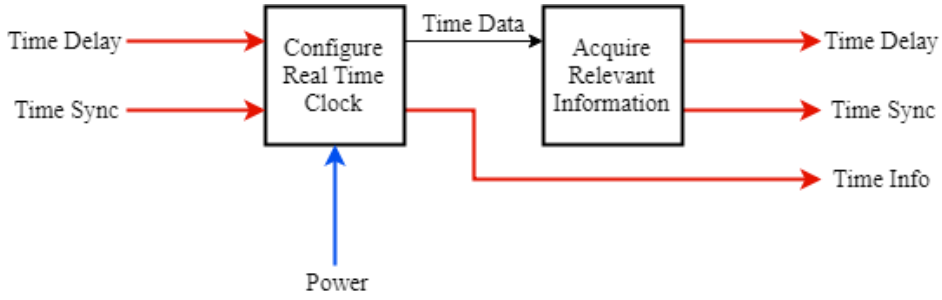


Figure 9: Level-2 Functional Decomposition of Time Synchronizing

Function: Control Processing

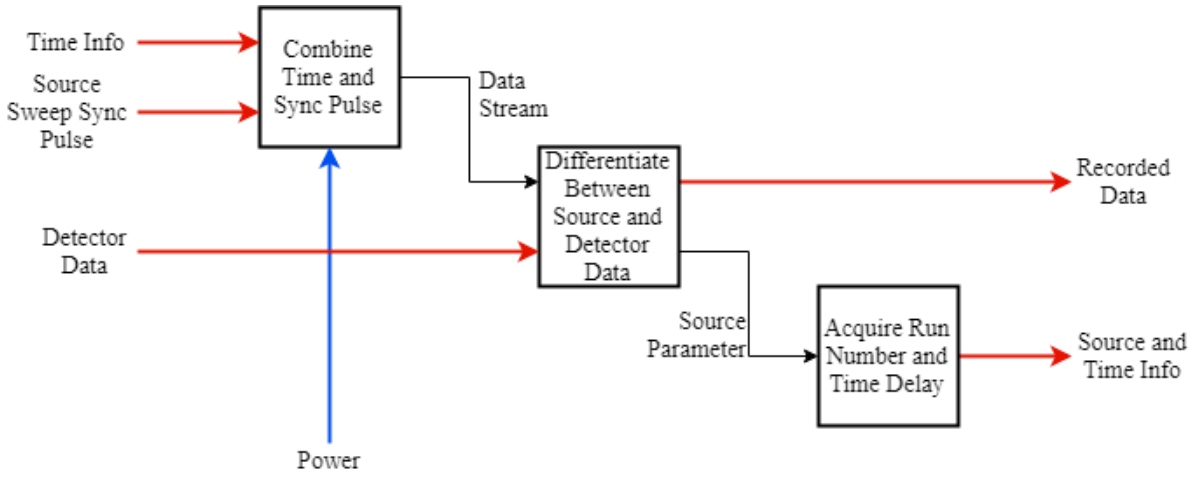


Figure 10: Level-2 Functional Decomposition of Control Processing

Function: Display Relevant Info

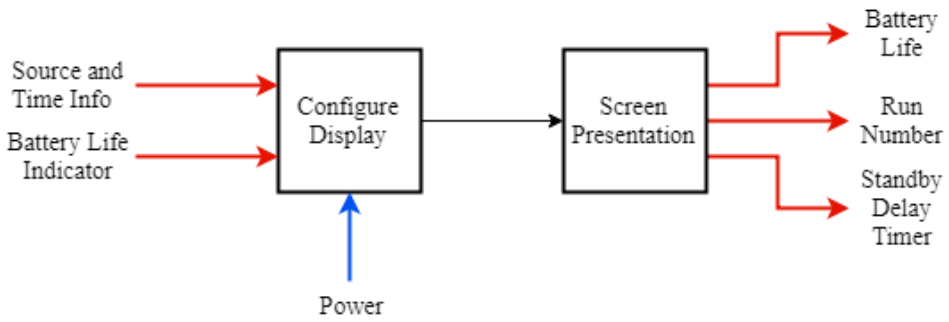


Figure 11: Level-2 Functional Decomposition of Display Relevant Information

4.3 Architecture of Detector Unit

4.3.A Physical Architecture

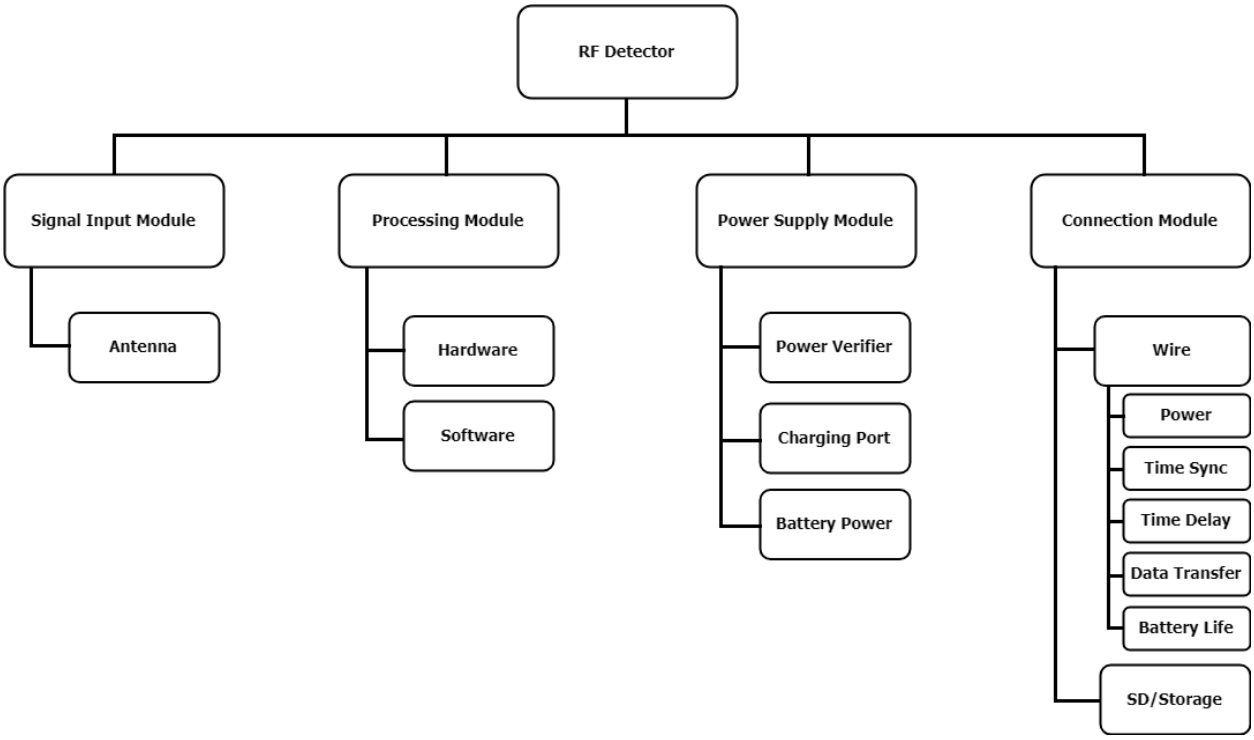
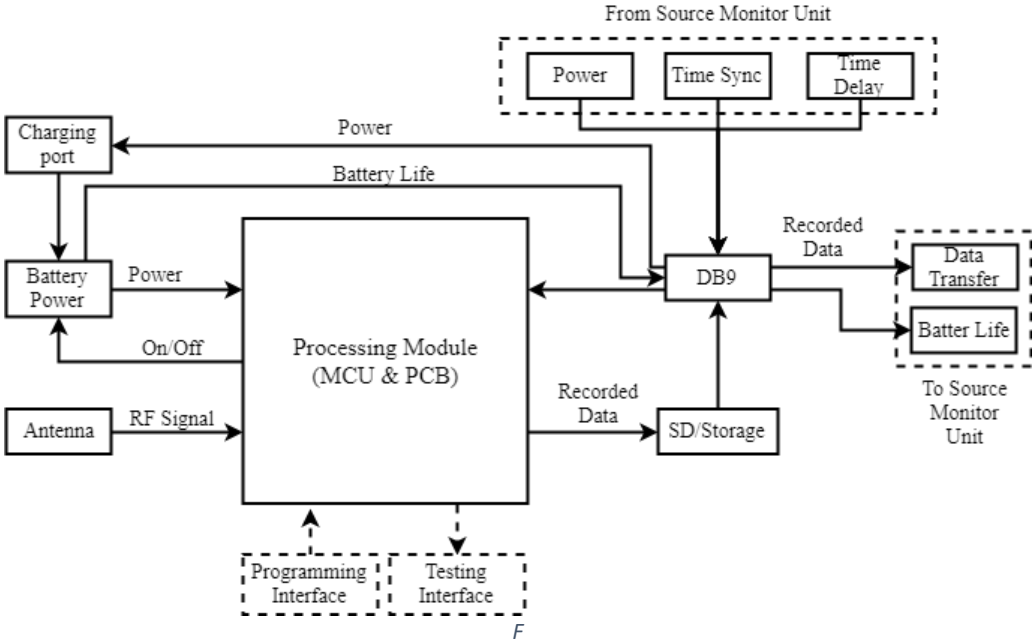


Figure 12: Physical Architecture of Detector Unit

4.3.B System Architecture



F

Figure 13: System Architecture of Detector Unit

4.4 Architecture of Source Monitor Unit

4.4.A Physical Architecture

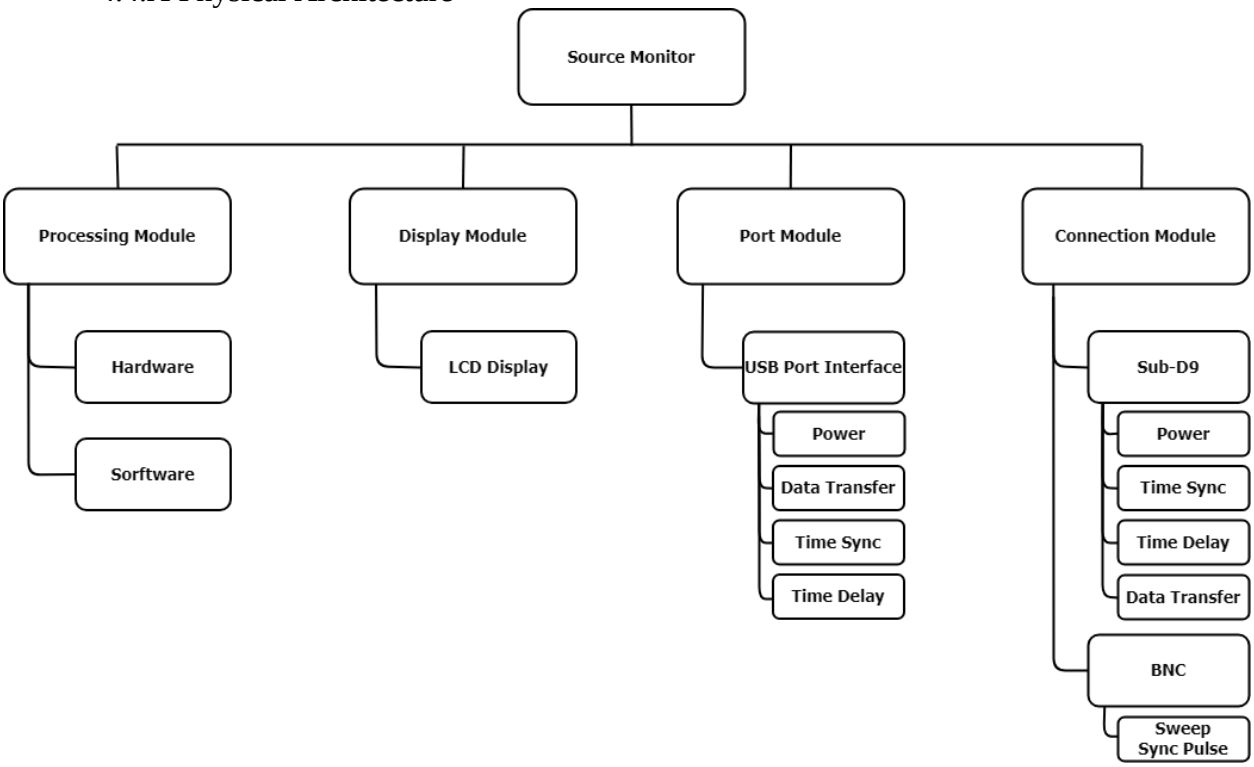


Figure 14: Physical Architecture of Source Monitor Unit

4.4.B System Architecture

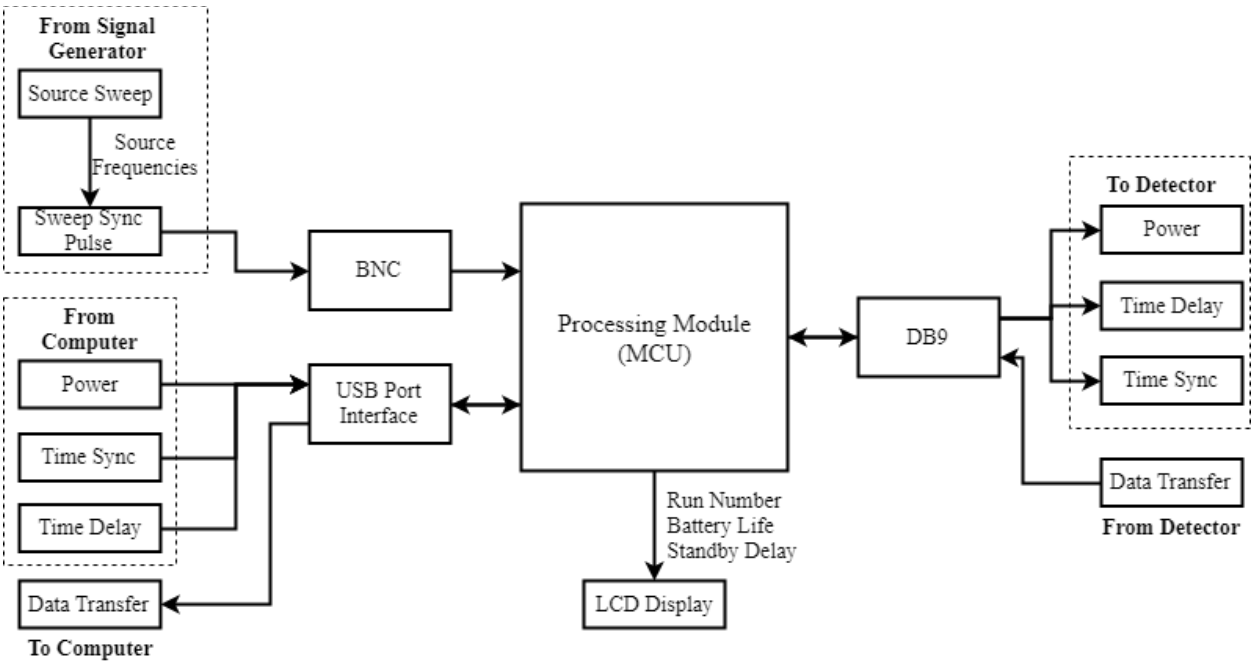


Figure 15: System Architecture of Source Monitor Unit

4.5 System Setup

Prior to the placement of the detector unit inside the enclosure, the detector unit is connected to the source monitor unit via SUB-D9, which is connected to the source computer via USB as displayed in *Figure 16*. The source computer provides power along with time sync and time delay that is set by the user, and the source monitor passes all three parameters to the detector unit. Detector unit charges while both units' time are synced with time delay set. During recording, detector unit is detached and put in the enclosure as exhibited in *Figure 17*, and after time delay initiation, the detector unit records the data while the source monitor unit records the sweep sync pulse via BNC. After the operation, detector unit is connected back to the source monitor unit as shown in *Figure 18*. Power is supplied to the detector unit for battery charging, and the recorded data from the detector unit is passed to the source monitor unit. The source monitor unit passes its own data along with detector unit's data to the source computer. The amplitudes, timestamps, and frequencies are combined to present the final data.

4.5.A Pre-Recording Setup

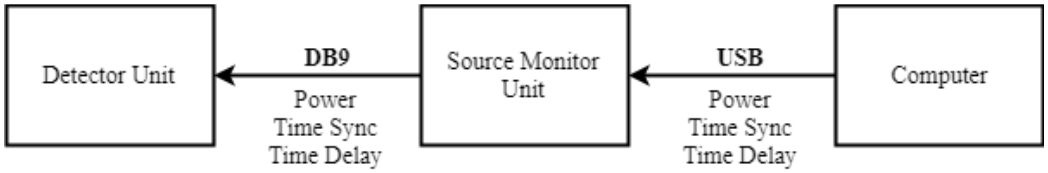


Figure 16: Pre-Recording Setup

4.5.B During Recording Setup

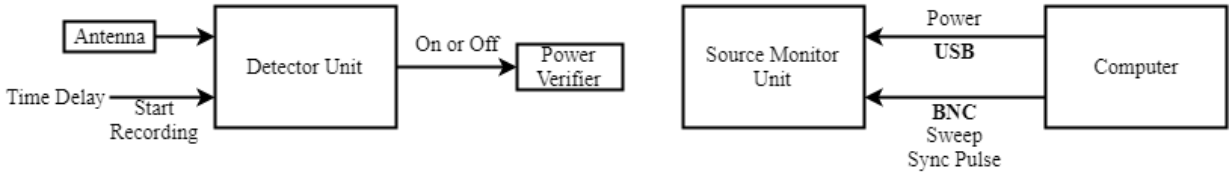


Figure 17: During Recording Setup

4.5.A Post-Recording Setup

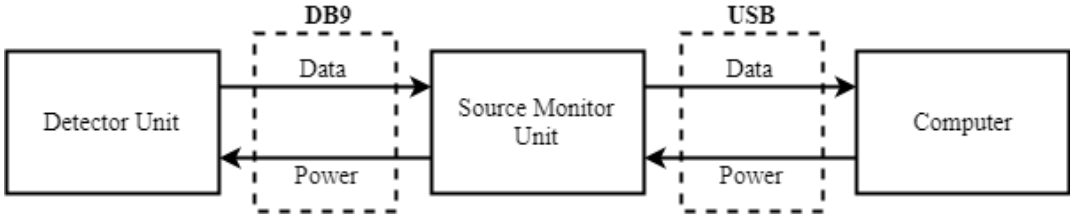


Figure 18: Post-Recording Setup

4.6 Hardware Schematic

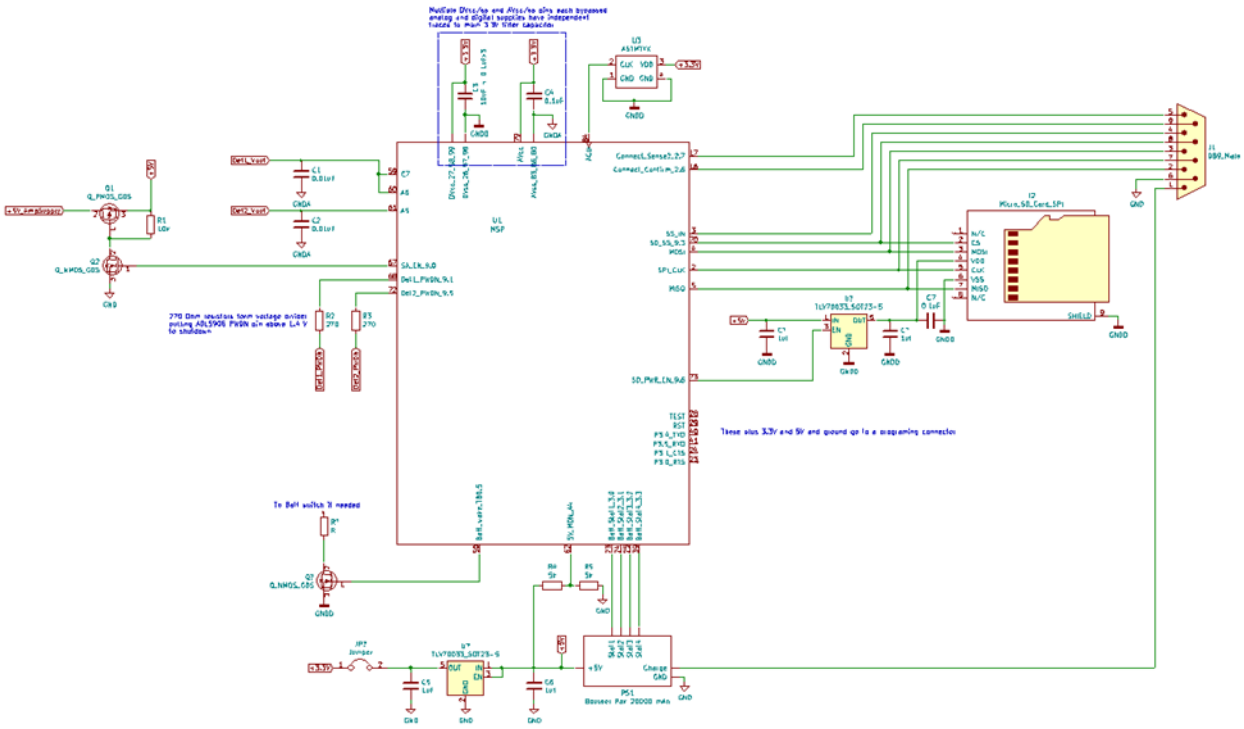


Figure 19: Detector Unit MSP Schematic

Figure 19 displays the circuit design for the MSP of the detector unit. The various power supply pins of the MSP microcontroller are bypassed to their appropriate analog or digital grounds. The analog inputs from the two RF detectors are locally bypassed by 0.01µF capacitors to reduce noise. The 5-volt supply to the RF amplifiers is sourced through a P-channel MOSFET. MOSFET technology was chosen over BJT technology to minimize the on-state voltage drop. This transistor's bias is controlled by a pull-up resistor and an N-channel MOSFET to allow the 3.3-volt signal from the MSP to control the 5-volt line. The two detectors are powered down by pulling the TADJ/PWDN pin above 1.4 volts. The 270 Ω resistors reduce the current consumption of the shutdown signals and provide some noise isolation for the TADJ voltage.

When the detectors are to be powered on, the shutdown pins on the MSP are placed in a high-impedance state. A voltage divider reduces the 5-volt supply to 2.5 volts which is fed to the analog comparator in the MSP to detect low voltage conditions. The 32 kHz clock signal is generated by a temperature compensated high precision oscillator. An external clock source was chosen, as opposed to using the crystal resonator driving circuit integrated into the MSP, because

the accuracy of the clock source for the real-time clock is critical for accurately determining the frequency that was transmitted during each measurement.

Designing a crystal oscillator circuit with proper capacitive loading and software-controlled temperature compensation was considered to high risk given the project timeline and availability of an inexpensive alternative. The measurement data gathered by the detector MSP is written to a micro-SD card via SPI and is read by the source monitor via SPI. A check sum value is calculated every sixty-three samples and written to the SD card to ensure data validity. The interface connector to join the source monitor and the detector is a standard DB-9 connector. An RF shield is available to prevent the RF environment from coupling into the detector circuitry when the devices are disconnected during a test. Connections are available for the SPI interface including slave select for the SD card and the detector MSP. Additional connections are used for power the charge the battery and to determine if the devices are connected.

The connection sense pin is configured as a digital input with an internal pull-down resistor. When the devices are connected, this line is pulled high signaling the detector MSP to reconfigure as an SPI slave to prevent to masters from driving the SPI bus. Once this is complete, the detector drives the connect confirm line, signaling the source monitor MSP it is safe to drive the bus. The battery to power the detector is a USB based portable power pack with pass through charging capability. It has charge management circuitry built in and includes a 5-volt power supply. The status signals originally used to drive LEDs on the power pack are connected to digital inputs on the detector MSP, so that it can monitor the charge status. A 3.3-volt low drop-out regulator is used to provide the power needed for the MSP, SD card, and the high precision oscillator. While its voltage regulation accuracy is important, it is not critical to analog voltage measurement accuracy, which uses the internal voltage reference source in the MSP.

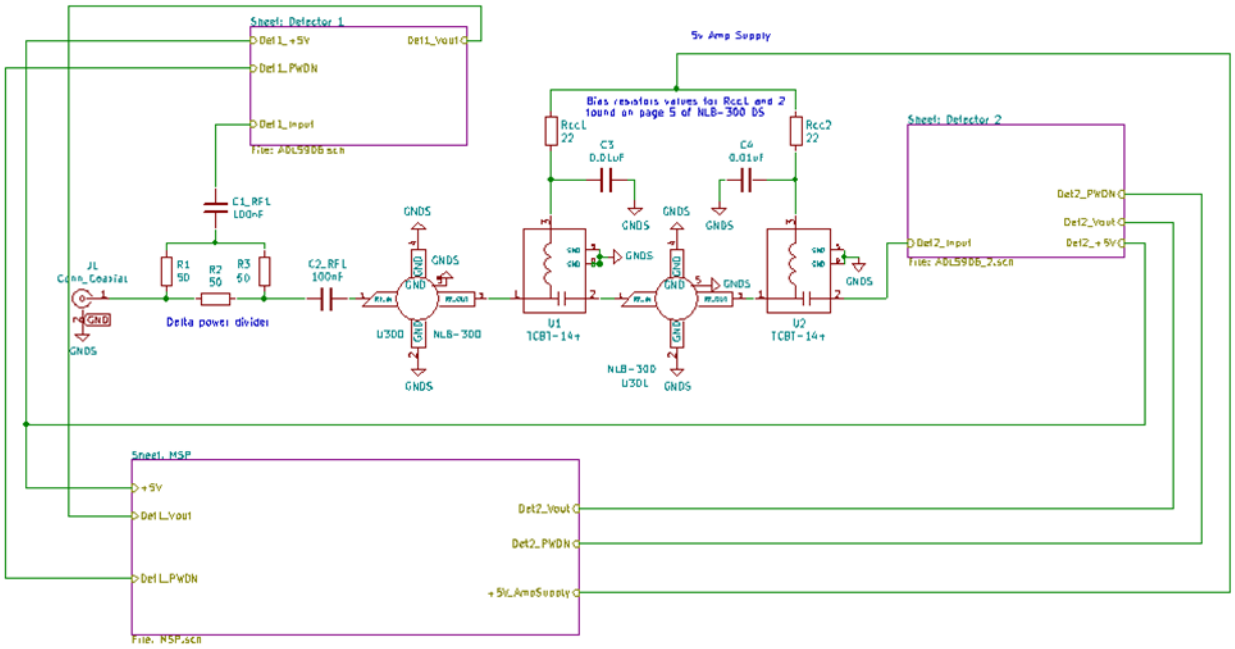


Figure 20: Detector Unit Schematic

Figure 20 exhibits the circuit design for the detector unit. A standard SMA coaxial connector is used for the RF input signal. This signal is split equally between the low gain detector input and the low noise amplifier input using a 6-dB resistive divider. A resistive divider is used despite its inherent power inefficiency because of its broadband frequency response. A reactive 3 dB power divider with even division and high return loss would be far more difficult to design. A delta resistive divider was chosen over a star divider due to the greater availability of 50 Ω resistors compared to 16.3 Ω resistors. Each NLB-300 provides fixed gain and are cascaded so that the total gain is a large portion of the dynamic range of the detectors, maximizing the increase to the system dynamic range provided by the two gain stages. DC power is provided to the amplifiers by biasing the output lines. Bias tees are used to isolate the DC power from the RF signal. The 22 Ω common collector resistors are used to set the operating point of the amplifiers.

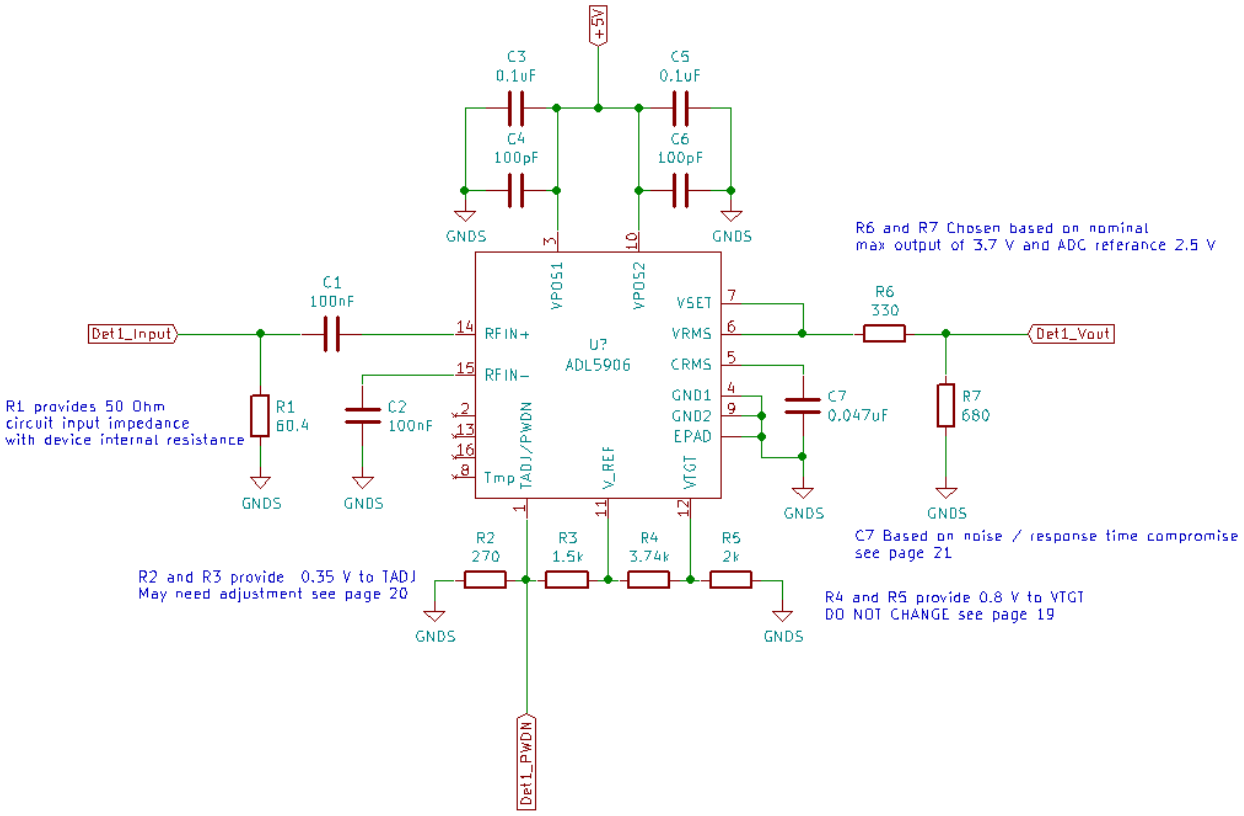


Figure 21: ADL5906 (detector chip) Schematic

Figure 21 shows the circuit design for the detector chip. The ADL5906 produces an analog output voltage that is linearly proportional to the RF power received in dBm. The 60.4 Ω input shunt resistor provides a 50 Ω input match when combined with the internal input resistance of the ADL5906. Capacitor C1 provides DC blocking for the bias on the input line generated by the ADL5906. Capacitor C2 provides a ground path for the RF signal from the negative differential input, allowing single ended operation for the unbalanced input. Resistors R2 and R3 divide the reference voltage, providing the temperature adjust set voltage. Resistors R4 and R5 divide the reference voltage, providing the squaring amplifier gain setting. Capacitor C7 provides output voltage averaging, the value chosen provides a compromise between noise immunity and response time. Resistors R6 and R7 divide the output voltage producing a voltage from 0 to 2.5 volts from the 0 to 3.7-volt output signal. This is to keep the analog voltage within the range of the ADC in the MSP.

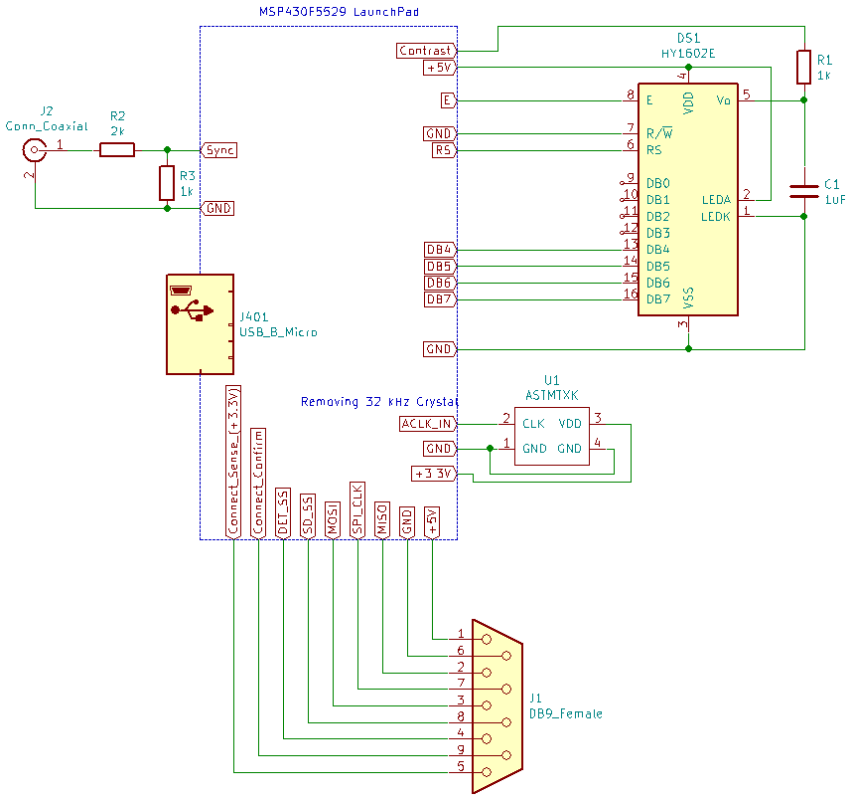


Figure 22: Source Monitor Unit Schematic

Figure 22 displays the circuit design for the source monitor unit. The MSP430F5529 LaunchPad is used as the control board in the source monitor. The LaunchPad already has a 3.3-volt regulator and proper bypassing for the MSP. It has the micro USB connector needed to interface with the test computer, and it has pin headers to connect to the 1602 LCD and the interface connector.

4.7 Software Description

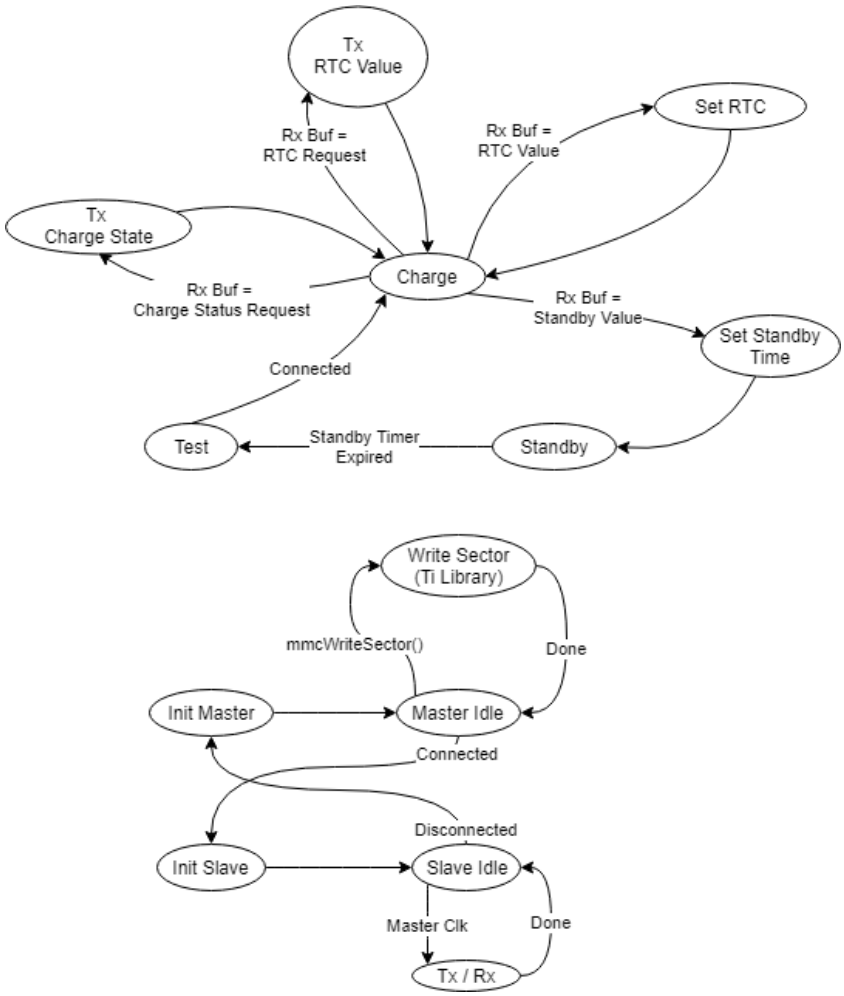


Figure 23: Main State Diagram of Detector Unit

When the detector is connected to the source monitor it is in the charge state. It is in SPI slave mode with the source monitor being the master. The source monitor will regularly poll the detector for the current charge state. The source monitor sends the test configuration parameters, being the current time and the standby delay time. When the detector is disconnected from the source monitor the standby timer starts. Once the standby timer expires, the detector changes to the SPI master in order to write data to the SD card. The ADC and RF amplifier are enabled as well as a sample timer interrupt. The detector remains in this state until it is reconnected to the source monitor.

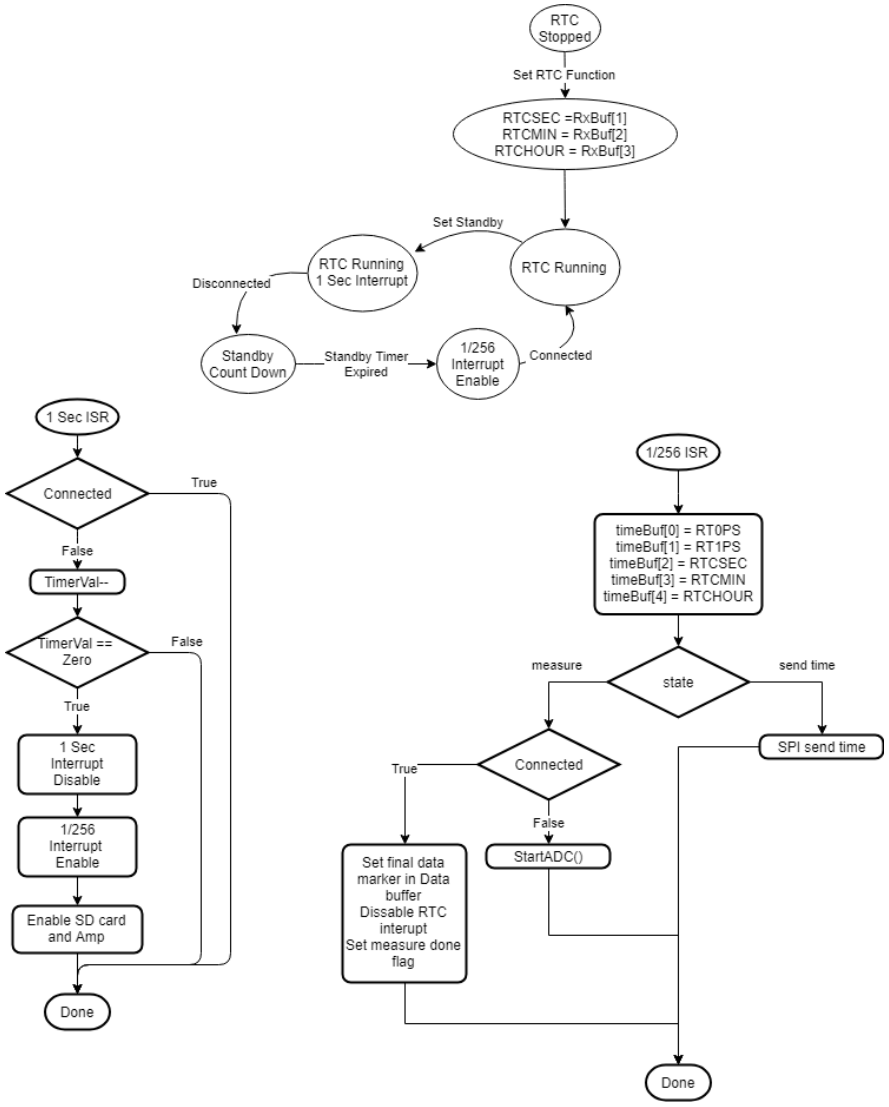


Figure 24: Detailed State Diagram and Flow Chart of RTC (Detector Unit)

Once the RTC is set, it runs continuously. When the detector is disconnected from the source monitor, the standby timer is started by enabling the one second interrupt from the RTC. While it is inefficient to use a one second interrupt to determine the standby delay as opposed to the RTC alarm peripheral, it allows code reuse from the source monitor, which uses the one seconds interrupt to update the LCD display showing the remaining time. Once the standby timer reaches zero, the one second interrupt is disabled, the ADC, detectors, and amplifier are enabled, and the sample timer is enabled by enabling the two-hundred fifty-sixth of a second interrupt. The sample timing interval is derived from the RTC prescaler, so it will be synchronized to the other RTC values. When the interrupt triggers, if the detector is in the measure state and the

devices are not connected, the RTC values are stored in the buffer, and the ADC sample is triggered. If the devices are connected, the final value marker is added to the data buffer, the measure done flag is set, and the RTC interrupt is disabled. If the detector is in the get time state, the current RTC value is written to the SPI transmit buffer and the RTC interrupt is disabled.

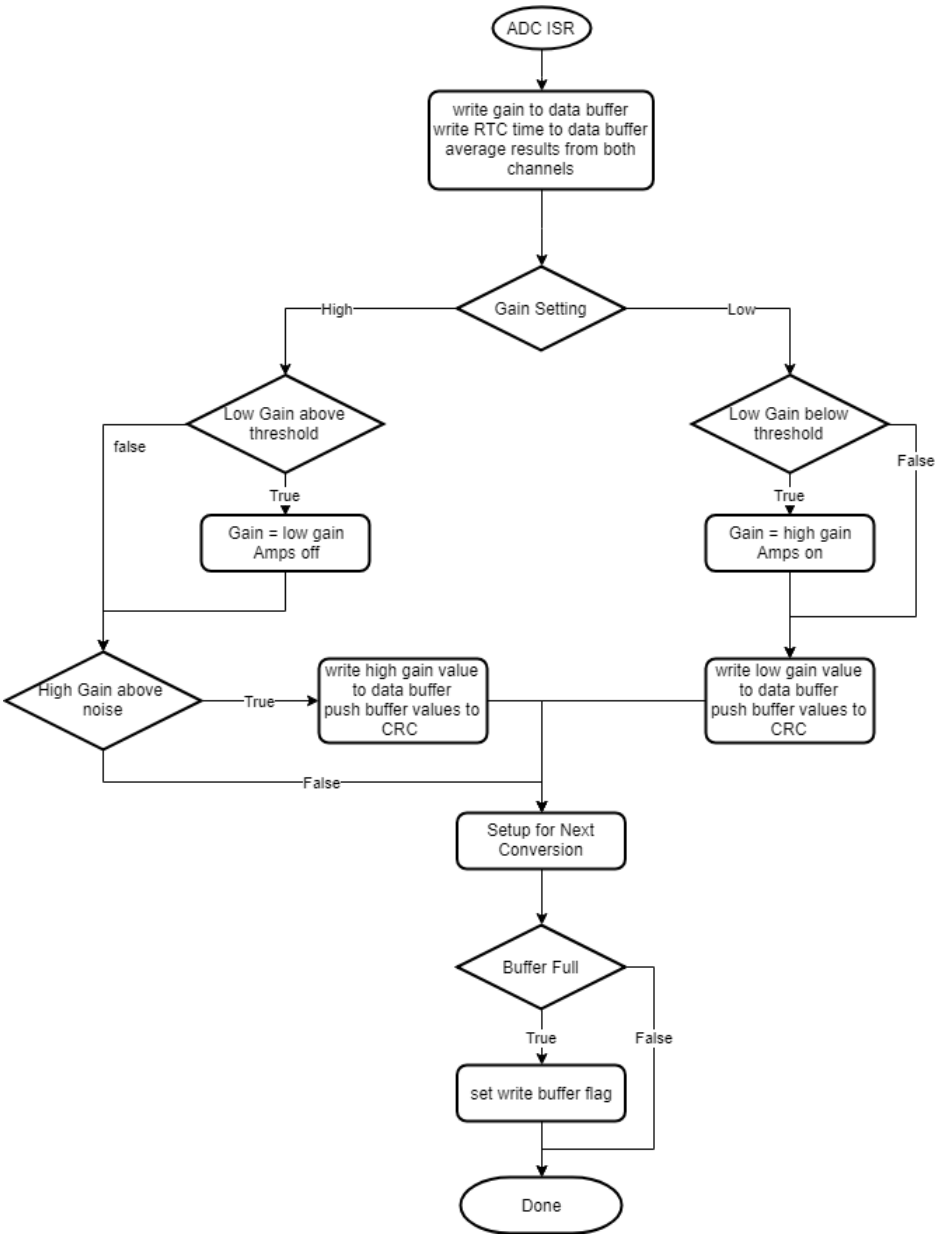


Figure 25: Detailed Flow Chart of ADC (Detector Unit)

When the sample timer ISR calls the StartADC function, the ADC is triggered via the software trigger bit. Four samples are taken from both the high gain and low gain channels. When the conversion is complete the ADC ISR is triggered. The ADC ISR averages each set of four samples by summing and right-shifting by two bits. The gain setting for the next sample is set based on the value of the low gain channel. If the gain setting is currently low and the reading is below the low-to-high transition threshold, the amplifier is turned on and the next reading will be recorded from the high gain channel. If the current gain setting is high and the low gain value is above the high-to-low threshold value, the amplifiers are turned off and the next reading will be from the low gain channel. When in the high gain mode, values are only recorded if they are above the noise threshold. Values written to the data buffer are also pushed through the CRC generator to create the check sum value. If the data buffer is full, the write buffer flag is set and low power mode is disabled to allow the main function to write the data to the SD card.

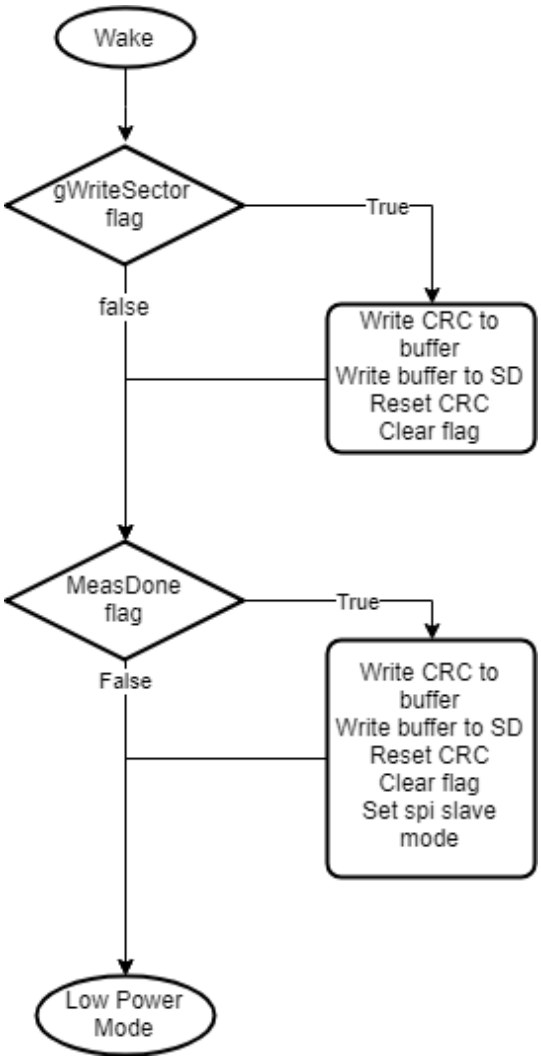


Figure 26: Detailed Flow Chart of Main Function (Detector Unit)

. When the data buffer is full the low power mode is disabled, the main function writes the CRC code for the current sector to the last position in the buffer and the sector is written to the SD card. This process may take longer than the time until the next measurement, but the data in the beginning of the buffer that will be overwritten will already be loaded into the SD card with a safe time margin. When the measure done flag is set by the reconnection to the source monitor, the last sector is written to the SD card, the detector is set to SPI slave mode, and the connection confirm signal is asserted.

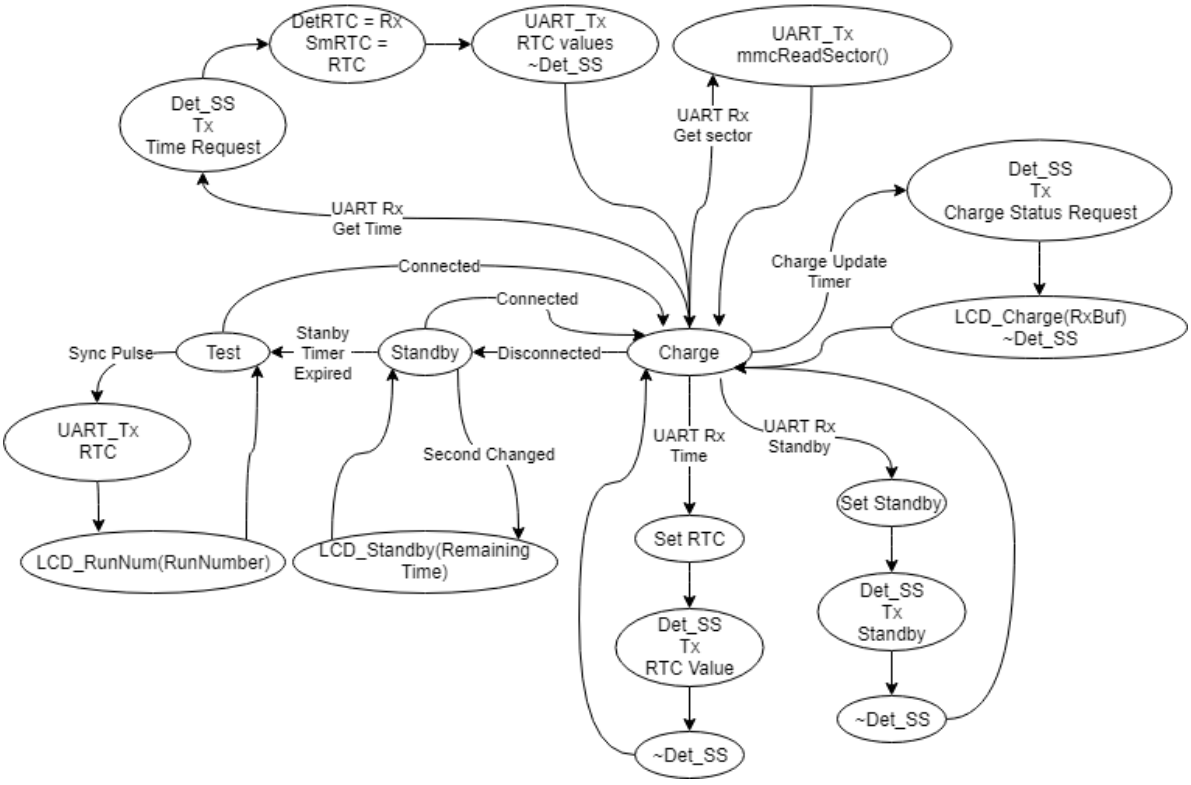


Figure 27: Main State Diagram of Source Monitor Unit

When the detector and source monitor are connected, the source monitor is in the charge state. It polls the detector for the current charge status at regular intervals (every second) and updates the LCD with the current state of charge. When a command arrives from the test computer via the emulated COM port, it is placed in the UART_Rx FIFO buffer and the source monitor is taken out of low power mode. If the command is to set the RTC, the time value provided by the test computer is loaded into the RTC registers and sent to the detector via SPI. Following the time value, the standby delay is sent form the test computer and is again passed to the detector. When the devices are disconnected, the standby timer is started. The amount of time remaining in standby is displayed on the LCD and updated each second. When the Standby timer expires, the source monitor changes to the test state. The time, from the RTC, of each rising edge on the sync pulse input pin is transmitted to the host computer. The LCD displays the number of pulses received to compare the run number detected with the run number transmitted. When the devices are reconnected, the source monitor returns to the charge state. When the source monitor receives a data request from the test computer, it retrieves the detector RTC value and stores a

copy of its own for clock drift detection. It transmits these values to the test computer and then uploads the data recorded on the SD card to the test computer.

The 1602A LCD is controlled using libraries provided by the University of Texas El Paso. The emulated COM port via USB in the MSP430F5529 is controlled using the Simple USB Back Channel libraries provided by Texas Instruments.

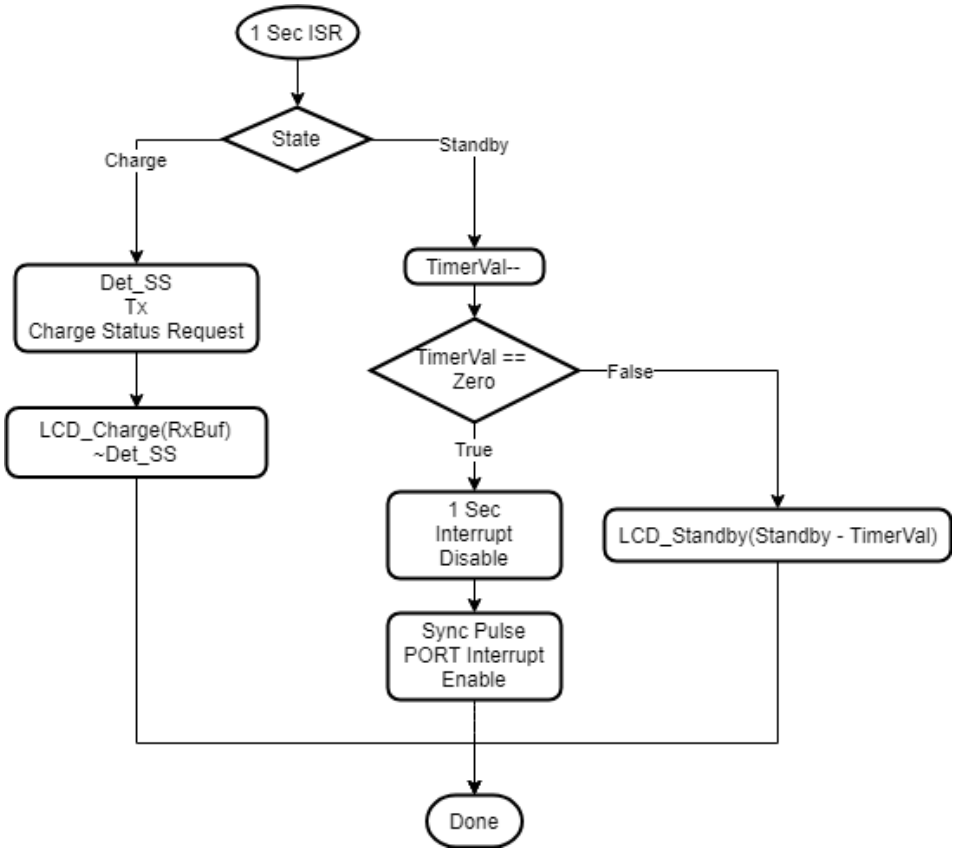


Figure 28: Detailed Flow Chart of RTC (Source Monitor Unit)

The RTC peripheral is used to generate the time stamps of each received sweep sync pulse. It is also used to measure the standby delay, and the charge status update interval. While the RTC alarm peripheral could be used to determine the standby delay, a separate timer interrupt would need to be used to regularly update the time remaining on the LCD.

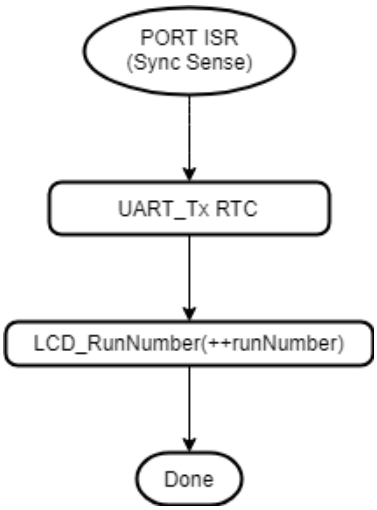


Figure 29: Detailed Flow Chart of Port (Source Monitor Unit)

The sweep sync pulse from the signal generator will trigger an interrupt that pushes the current RTC value into the UART transmit buffer and updates the run number on the LCD.

5. Experimentation

5.1 ADC Module

The ADC module in the detector was tested by issuing a sample command from the host computer to the source monitor via the UART interface, the sample command was passed to the detector via SPI, the detector would initiate an ADC acquisition, and return the result to the host computer through the reverse path. Different voltage signals, 0.5 V, 1 V, 1.5 V, and 2 V, were applied to the ADC channel input, and 128 samples were collected for each voltage signals and plotted. The ADC was first configured to take a single sample with a wide sample period. It was then configured with reduced sample period that allowed eight samples to be taken in the same amount of time, and the values were averaged per trigger, which improved the results.

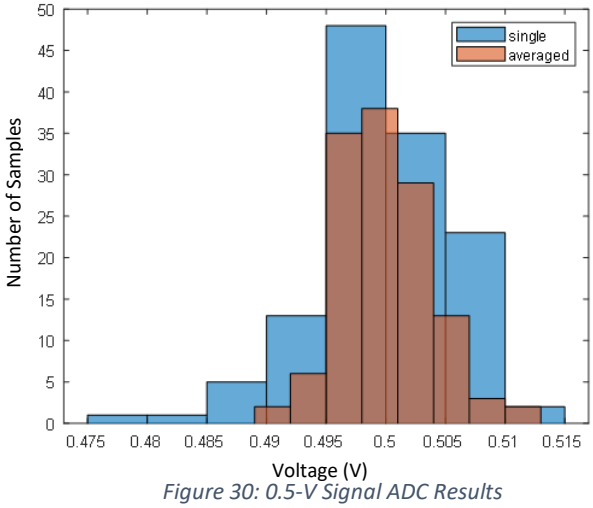


Figure 30: 0.5-V Signal ADC Results

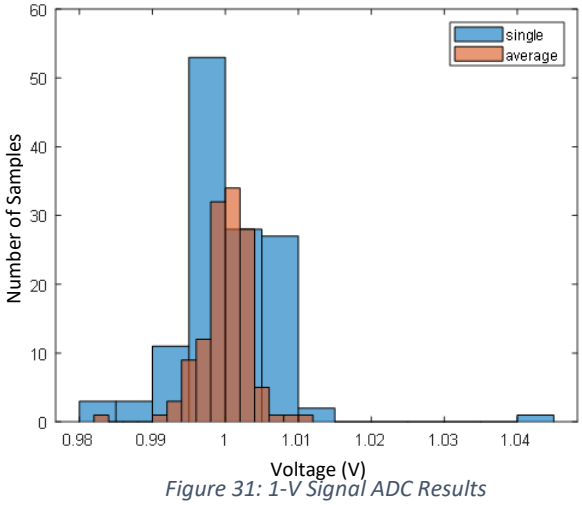


Figure 31: 1-V Signal ADC Results

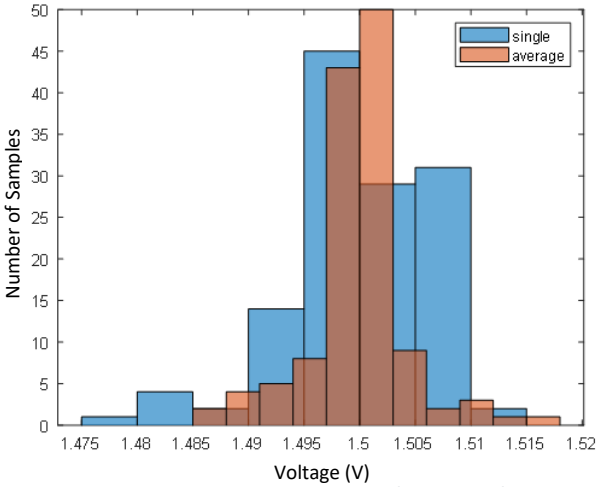


Figure 232: 1.5-V Signal ADC Results

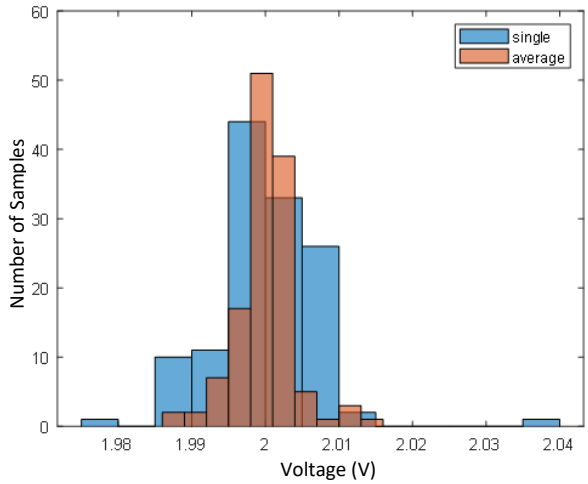


Figure 33: 2-V Signal ADC Results

5.2 RTC and ADC Integration

The ADC module was integrated with the RTC. This allowed sample times to be synchronized to the RTC and have a regular sample rate of 256 samples per second. A 256-sample buffer containing ADC values and their respective timestamps is populated when commended by the host computer. The modules were then tested as follows: A two channel arbitrary waveform generator was used to provide one second sync pulses to the source monitor sweep sync input and a synchronized sinewave to the detector ADC input. The detector was configured to only store ADC values above 0.6 volts to create disjoint sets of samples. The RTCs were set to the system time of the host computer, the RTC values were then immediately read back providing a reference skew, detector sampling was enabled and sweep sync monitoring was enabled, after two sweep sync pulses are detected the sync pulse detection is disabled, after a delay the sample buffer is read from the detector, finally the RTC values are read to determine the final skew. The RTC values read from the source monitor are normalized to the two sync pulses space one second apart. The normalized RTC values from the source monitor are used to normalize the detector sample times based on the pretest and posttest RTC values. The time values are then slid so that time zero aligns with the first sweep sync pulse. The samples (orange crosses) were then plotted over the theoretical values (blue trace).

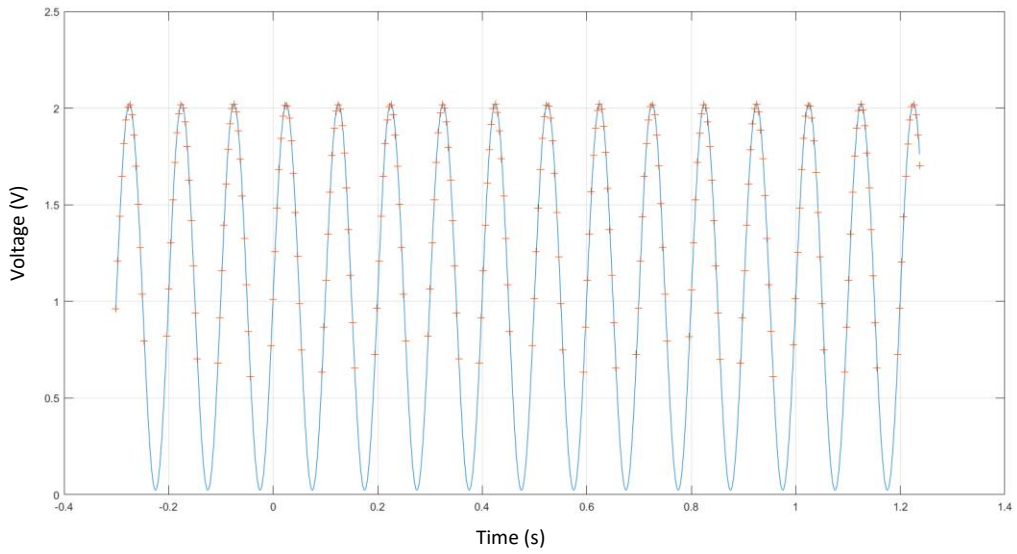


Figure 34: 1-V 10-Hz Signal with Data Points Plotted

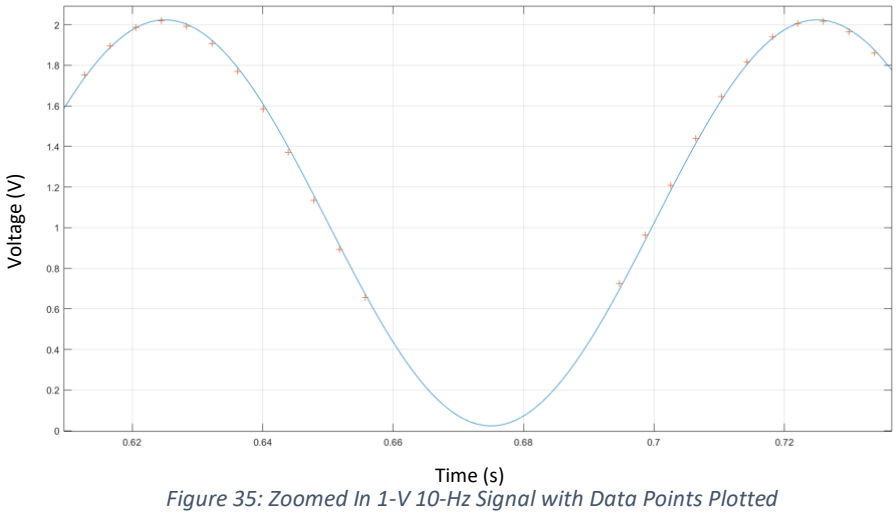


Figure 35: Zoomed In 1-V 10-Hz Signal with Data Points Plotted

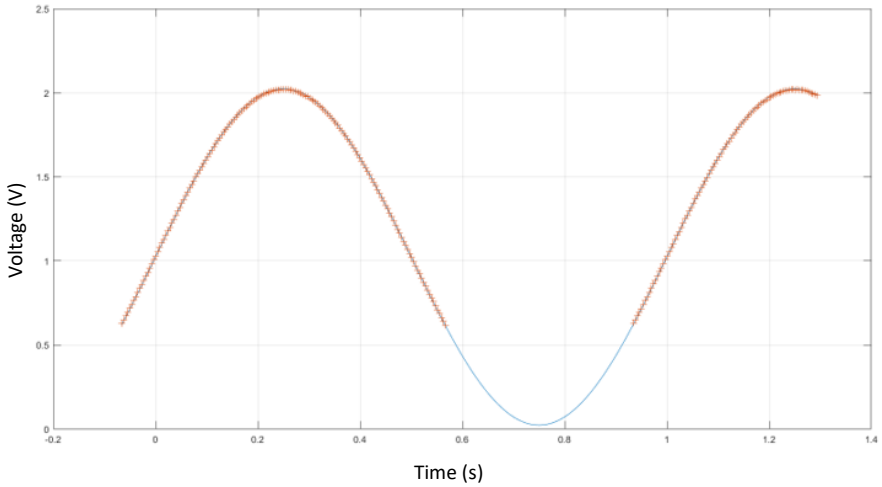


Figure 36: 1-V 1-Hz Signal with Data Points Plotted

5.3 DC Offset

Small DC corrections needed to be made to the theoretical waveforms to align them to the samples. To determine the necessary offset value, the sinewave input was replaced by a 1-volt DC input as shown below.

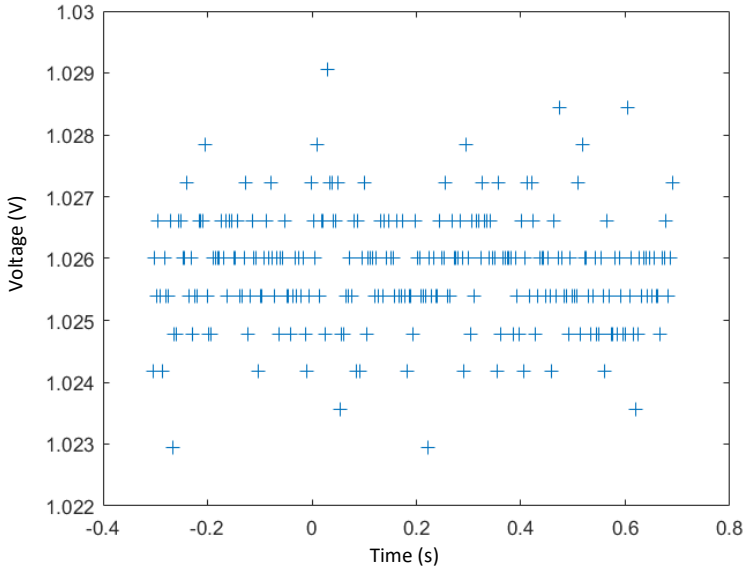


Figure 37: 1-V Input with Data Points Plotted

There was about a six-millivolt spread in the ADC samples. This and the DC offset led us to measure the DC reference voltage with an oscilloscope. Not only is there a DC offset, but there is intermittent noise of about five millivolts.

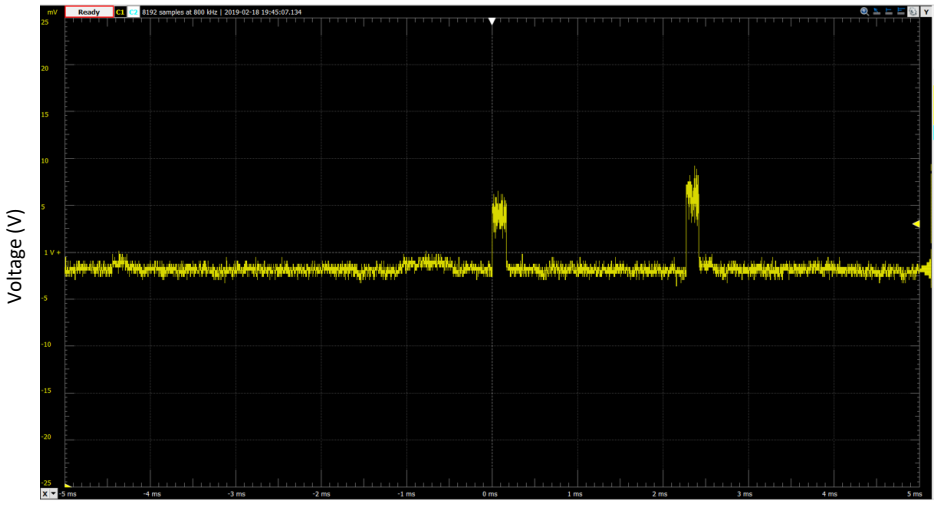


Figure 38: Oscilloscope Displaying Noise

5.4 RTC Skew

RTCs of the detector unit and the source monitor unit were synchronized and ran for timestamping for a duration of over 10 minutes. The experiment was done to see if there are any notable differences in timestamp as devices are ran for a period of time. If there presents a skew of linear characteristic, the time difference can be easily countered to give correct synchronicity.

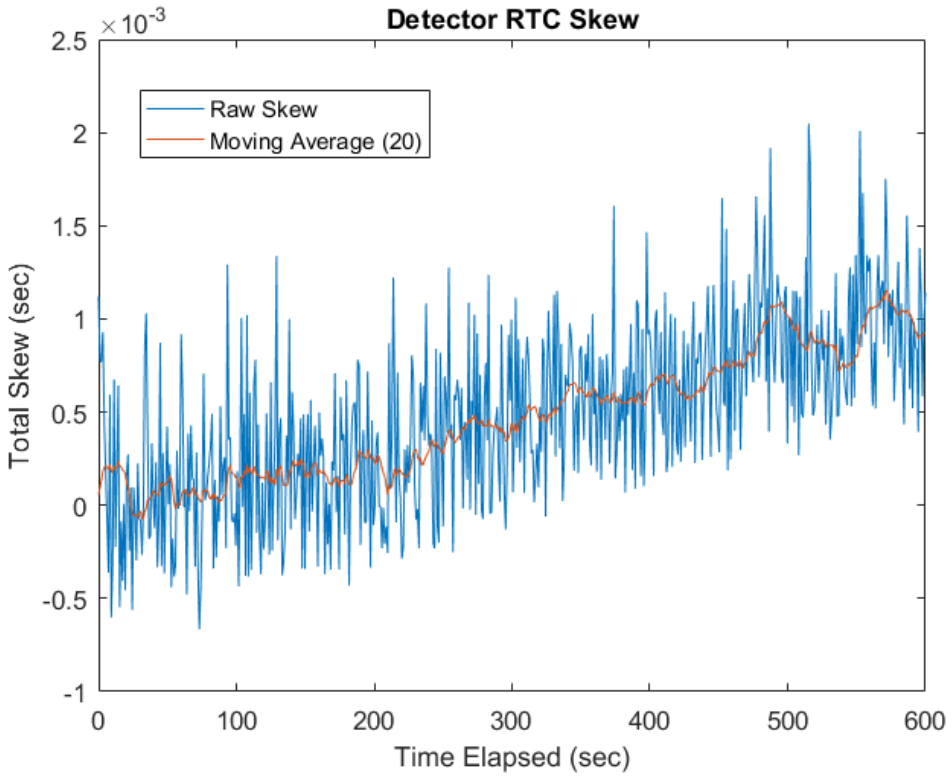


Figure 39: RTC Monitoring of Detector and Source Monitor Units

5.5 Writing/Reading SD Card

Figure 40 shows the result after writing to and reading from the SD card onboard the Detector Unit. A known ADC input signal was put into the MSP while varying the frequency. This was done for over 20 seconds to ensure that the data was indeed being stored in the SD card and not the internal storage of the MSP.

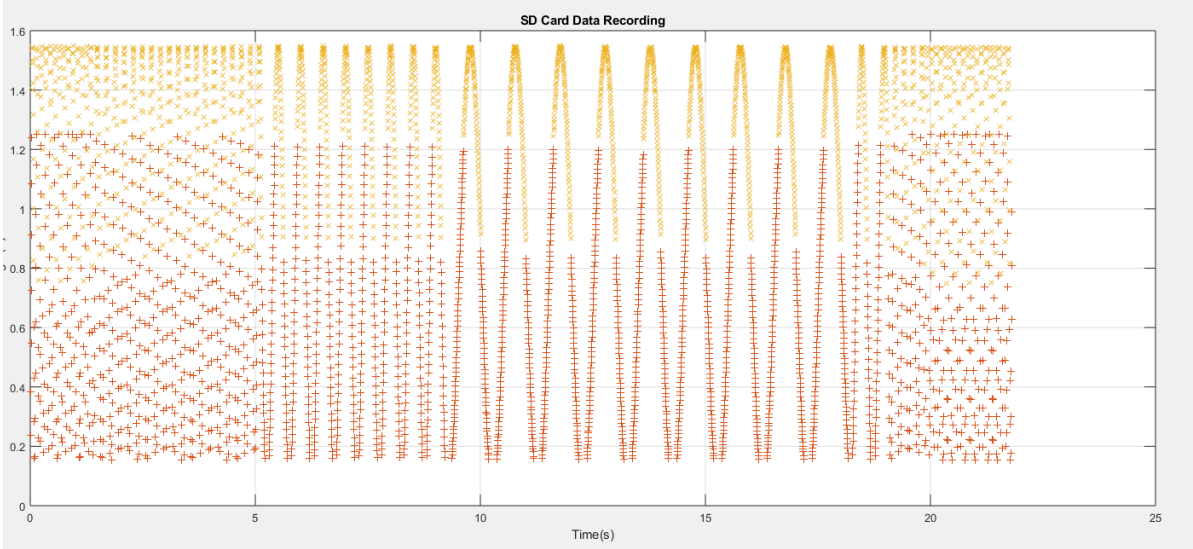


Figure 40: SD Card data recording output.

5.6 Power Response of Detector Unit

Figure 41 shows the power response for the low-gain channel of the Detector Unit as Input Power (dBm) vs. ADC Value. This data was acquired using a Keysight 8257D Analog Signal Generator, with high precision. Discrete samples were taken over the range of 100 MHz to 6 GHz, with input power between -50 dBm and 10 dBm.

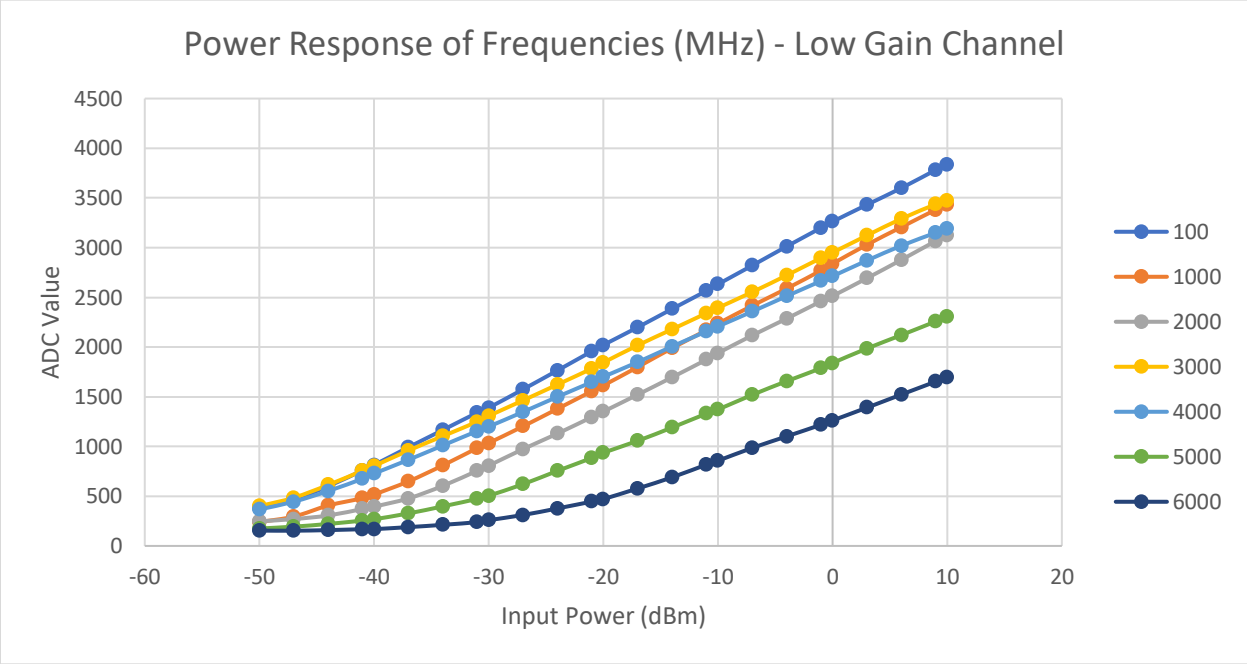


Figure 41: Power Response of Frequencies, low-gain channel.

Figure 42 shows the power response for the high-gain channel of the Detector Unit as Input Power (dBm) vs. ADV Value. This data was acquired using a SynthNV signal generator, which was not as precise as the device used for the low-gain channel. This was due to time constraints. Discrete samples were taken over 100 MHz to 4 GHz, with input power between -50dBm and 10 dBm where possible.

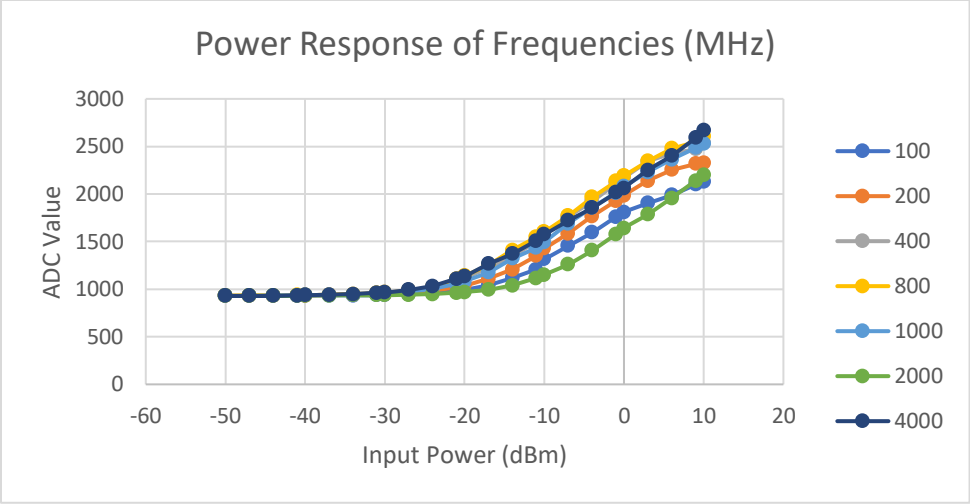


Figure 42: Power Response of Frequencies, high-gain channel.

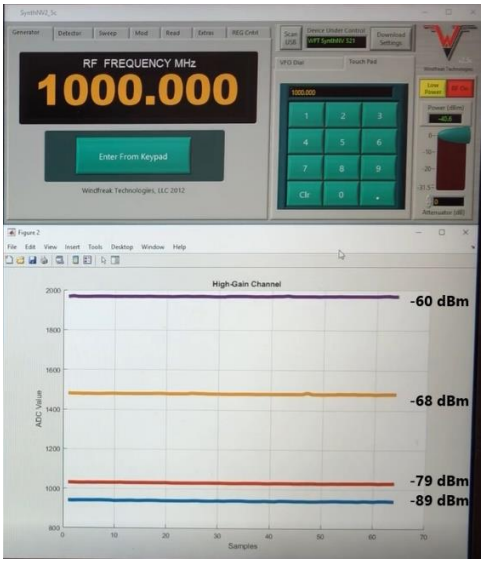


Figure 43: Power Response at 1 GHz, high-gain channel.

Figure 43 displays another occasion of testing high-gain channel power response at 1 GHz, where different power signals were inputted through the high-gain channel to exhibit the ADC values being stored.

5.7 Frequency Response of Detector Unit

Figure 44 shows the Frequency Response of the low-gain. This data was collected by inputting a constant power level and taking discrete samples at given frequencies, between 100 MHz and 6 GHz with the Keysight 8257D.

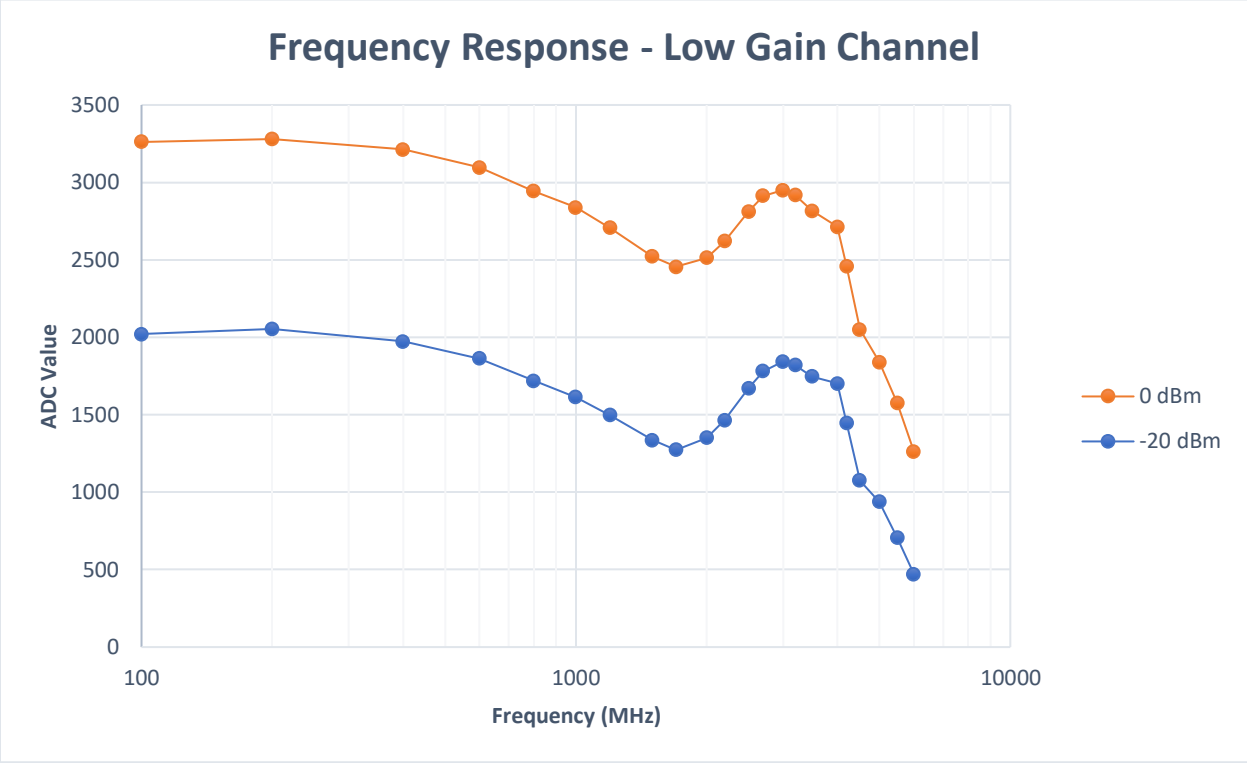


Figure 44: Frequency Response, low-gain channel.

Figure 45 shows the Frequency Response of the high-gain. This data was collected by inputting a constant power level and taking discrete samples at given frequencies, between 100 MHz and 4 GHz using a SynthNV signal generator.

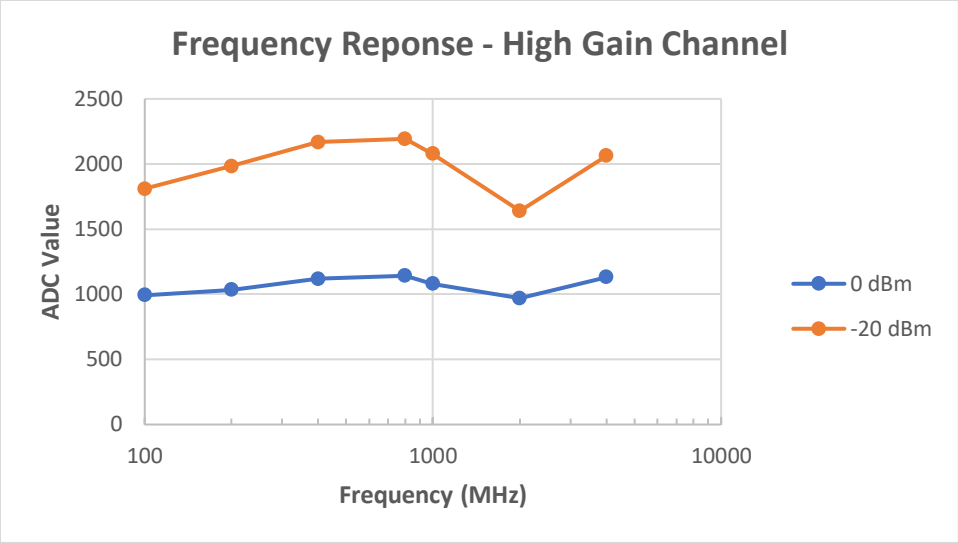


Figure 45: Frequency Response, high-gain channel.

5.8 Power Accuracy

Figure 46 shows the distribution of normalized ADC samples, tested at 6 GHz on the low-gain channel. This shows an accuracy of +/- 6 ADC values. *Figure 47* shows the power response of the low gain channel for a 6 GHz input. 6 GHz was chosen as it was the worst of our frequency responses, therefore it is the worst-case scenario. This plot has a slope of 41 ADC values/dBm. Together, this yields an accuracy of +/- 0.146 dBm.

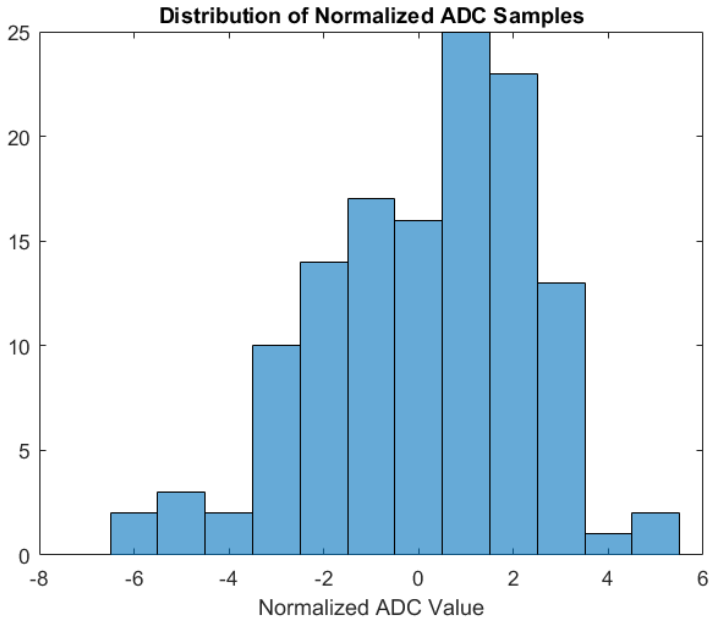


Figure 46: Normalized ADC distribution

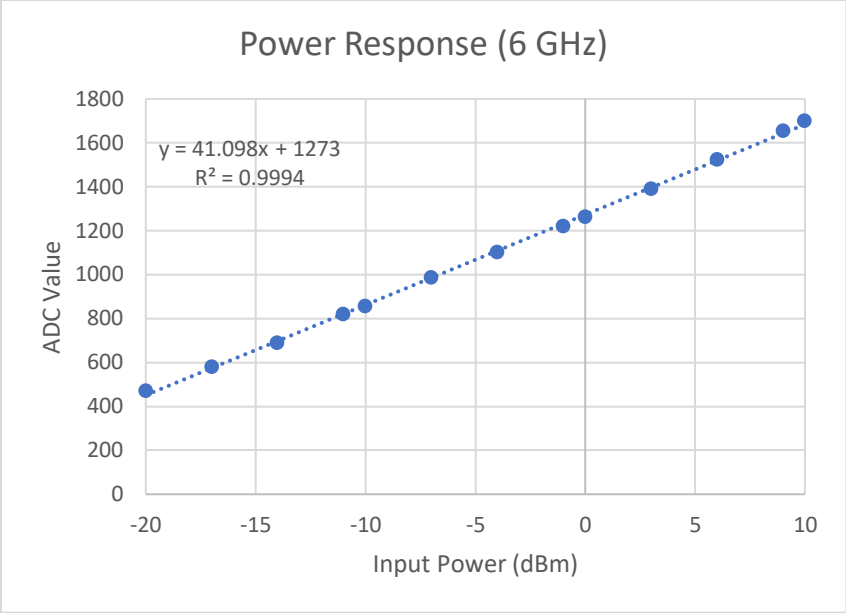


Figure 47: Power Response at 6 GHz, low gain channel.

5.9 Battery Power

In order to test battery power, the battery pack was first fully charged. After fully charging the batteries, the Detector Unit was left operating on battery power for a period of 8 hours. At the completion of the 8 hours, it was confirmed that the Detector Unit was still operating. For further confirmation, the battery pack's onboard LEDs indicated that there was still charge remaining in the battery pack.

6. Evaluation of Experiments

Sections 5.1, 5.6, and 5.8 tested the accuracy of the detector unit. As discussed in Section 5.8, we achieved an accuracy of +/- 0.146 dBm at 6 GHz which meets our required accuracy of +/- 2 dB. The reason 6 GHz was selected for this requirement is it is our worst-case scenario, since it is our poorest performing frequency.

Section 5.2 shows the ability of the Detector Unit to correctly match the amplitude of the acquired signal with the correct timestamp. This experimentation also verified that we were able to sample at 256 samples per second, exceeding the required rate of 230 samples per second. This data can then be stored on the SD card, to be read by the Source Monitor upon completion of testing. At 8 bytes per sample, with a 16 gigabyte SD card, this also meets our requirement for storage of 6.93 million samples.

Section 5.7 details the frequency responses of the Detector Unit. The 100 MHz to 6 GHz frequency requirement is met, although there appears to be some impedance mismatching in the circuit. This can be observed as a dip, rise, and drop in the higher end of the frequency range. Ideally, this response would be flat. We were expecting a drop off towards the end of the response due to our RF detector, but that does not completely explain the response. What likely caused this deviation is an impedance mismatch in the PCB design, possibly due to the material used as a substrate.

From the power responses found in Section 5.6, it can also be shown that the minimum detectable power is around -20 dBm for the low-gain channel. This is the point at which the 6 GHz response climbs above the highest noise level. If we were able to reduce the noise in the circuit, we would have been able to achieve the minimum detectable power goal of -30 dBm. With the high-gain channel, Figure 43 displays a significance detectable power from -60 dBm, which exhibits the systems ability to go down in minimum detectable power below the goal and increase the dynamic range. Unfortunately, during data gathering, combination of unknown error and unreliable signal generator caused the system to not respond well as such. Since the minimum detectable power was -20 dBm, the highest we tested was 10 dBm, which achieves our requirement of a 30-dB dynamic range.

Section 5.9 details the experimentation regarding battery life. After running the Detector Unit for 8 hours on battery power, we found that the Detector Unit was still operating.

Furthermore, as mentioned, the battery pack still indicated remaining charge. This verifies that the minimum battery life of 8 hours was achieved.

Although no experiments were conducted on the case for the Detector Unit, we successfully met the dimension requirement of 6”x6”x3”, as our enclosure size was 6”x3.24”x1.81”. Furthermore, as seen in the following figure, we were able to drill and mount an SMA connector on the enclosure, meeting the requirement to hook up to an SMA antenna. Similarly, the Source Monitor, as shown below, is able to interface with the Detector Unit, the sync pulse, and the controlling computer.

Together, these two devices have successfully met all requirements but the minimal detectable power. This prototype has successfully proven that this concept could work for the customer and replace the current method of shielding effectiveness testing.

Figure 48: The Detector Unit, from two different angles.

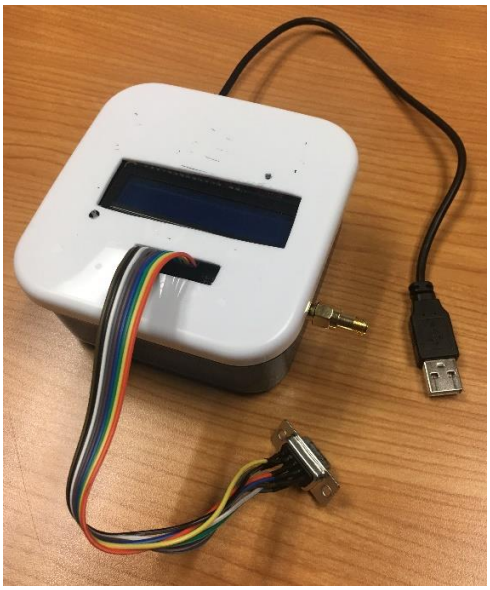


Figure 49: The Source Monitor Unit

7. Other Issues and Topics

7.1 Reason for the Project

This system was designed to replace the current method used for shielding effectiveness testing of a given enclosure for NSWC Dahlgren Electromagnetic Environmental Effects Assessment and Evaluation Branch, B52. As mentioned previously, the current method involves drilling a hole in the enclosure-under-test. This is not desirable for several reasons, including possibly compromising the shielding and the irreversible damage done to the enclosure sample. The RF Detector for Shielding Effectiveness Testing allows the customer to conduct testing without the need for drilling a hole in the enclosure, since the Detector Unit is a standalone, self-powering device that stores all collected data for later retrieval. If successful, this alternative to drilling holes will save time and money for the customer and their client who no longer leaves the test with a damaged product.

7.2 Potential use of the Project

The RFDSET system could have applications outside of the designed use. Although designed specifically for the testing required by the customer, another company or organization could have a testing procedure with similar specifications and use this product with little to no modifications. Since the customer will likely not make the results of these tests public, nor does it test enclosures that are not relevant to its mission, it is likely that another company or organization could make use of RFDSET for its own purposes. This system does not have a broad range of uses, even in the RF/Microwave community, as it relies on knowing exactly what frequencies, and at what power, the Detector Unit is being exposed to. Therefore, the applications would likely be limited to different forms of shielding effectiveness testing.

7.3 Cost Figures for the Project:

The materials for the project, not including the PCB and any spare components already in hand, cost around $300. The PCB fabrication, for three four-layer boards cost around $90. In total, around $390 were spent on materials. However, the true cost of this project is driven by the number of man-hours spent throughout the last two semesters. At $20 per hour, 845 man-hours, the total cost of the project becomes $17,290.

7.4 Alternatives to the Implemented Design

The PCB design and component selection were done by first-time designers, and surely leaves some room for improvement. The first area that could be implemented differently is the PCB shape and layout. A more experienced designer could save on total area of the PCB, cutting costs significantly at scale. Alternatively, the shape of the PCB could be modified to fit different specifications. For example, it may be laid out in a longer, yet less wide, form.

Choosing different qualities or sizes of components could impact both monetary and labor costs, as well as overall results. One direction of this would be to save money and sacrifice performance, and the other would cost more but improve performance.

More drastic changes to the overall design could shift the frequency range that this device operates in. However, this would not just require new components, but likely new PCB footprints, new schematic elements, new PCB material, and heavily modified software, to name a few changes.

7.5 Maintainability/Maintenance

The hardware components should be inspected periodically to ensure no components have come lose or been damaged. Wear-and-tear is expected on areas like the Detector Unit coaxial connector and similar connectors. The software should be maintained and possibly updated as well. One of our team members works for the customer and will be on hand to address software issues. Furthermore, all software used will be documented and provided to the customer.

7.6 Retirement/Replacement/Disposal

If components are found to be faulty or damaged and need to be replaced, replacement parts can be ordered by referencing the bill of materials and schematic. An experienced technician or engineer could replace the components directly on the PCB. More severe damage may call for a re-fabrication of the entire board. Replacement of the battery may also be required; in which case the lithium-ion batteries should be swapped for exact replacements. Disposal of the device should be conducted according to the standard operating procedure of the Department of the Navy regarding electronic waste, with special attention being paid to the lithium-ion batteries.

8. Administrative

8.1 Project Progress

Overall, the project progressed rapidly over the course of the two semesters. Despite the rapid pace, the workload of the project was significantly higher than expected. Some elements of the project were delayed, but most of the elements were completed on time.

The software development side of the project required a significant number of man-hours. However, the software team was able to consistently and reliably complete the necessary modules and interfaces within the allotted time. This was due to their persistence and dedication.

The hardware development side of the project required more time than originally allotted. Specifically, the PCB design stage was completed later than originally scheduled. This was due, in part, to changes in the schematic. However, the main reason for the delay was that the hardware team underestimated the complexity of the PCB design process. Selecting or creating footprints for each component was the first contribution to the setback. Some components required the team to diligently create footprints, which required attention to detail and a lot of time. Next, placing PCB components and routing signals delayed the process even further. Once the PCB design was complete, however, the quick fabrication and delivery of the boards from the vendor helped to make up for some lost time. The quick PCB assembly by the team also made up for some lost time, as that task was delayed significantly by the PCB design delays.

8.2 Task Completion

Power Supply Development:	Battery Power Design – Complete
	Power Connection Setup – Complete
Hardware Development:	RF Detector Setup – Complete
	Amplifying Stage Setup – Complete
	PCB Design – Complete
	PCB Assembly – Complete
Software Development:	UART Interface – Complete
	Memory Module – Complete
	LCD Interface – Complete
	Communication Module – Complete
	RTC Module – Complete
	PORT Module – Complete
	ADC Module – Complete
	RTC ADC Integration – Complete
	Battery Monitor Module – Complete
	Standby Timer – Complete
	Checksum – Complete
	System Integration – Complete
Final Testing:	Complete

8.3 Changes Made

Throughout the progress, some aspects were changed. For example, rather than having gain stages that were independently enable or disabled throughout the course of the test to increase minimal detectable power, we elected to have two separate signal paths, one with no gain and the other with high gain. The reason for this change was the time it took the amplifiers to power on or off when needed was an issue that we elected to avoid. Another change was the stripline method of PCB trace impedance matching was swapped out for the grounded coplanar waveguide in order to have better control over the trace dimensions.

8.4 Extra Activities

Regarding extra activities besides planning and executing that plan, the team ended up dedicating a large amount of time just researching different principles. Since the RF and Microwave range of the electromagnetic spectrum presents complicated issues in circuit design, the team had to thoroughly research and understand some principles involved (such as impedance matching) that were crucial to the success of our project.

8.5 Funds Spent:

Components- $300

Four-layer PCB - $90

Total: $390

8.6 Man-hours Spent

Kevin Riley – 250 Hours

Shahed Afrad – 185 Hours

David Phelps –200 Hours

Steve Kim – 210 Hours

Total: 845 hours

As discussed in the contributions subsection of the Approach, Kevin Riley spent a significant amount of time developing the software for this project, in addition to the design of the project and communication with the customer. Shahed Afrad spent his time between software, component selection, and PCB soldering. David Phelps and Steve Kim spent their time between PCB design, administrative tasks, and component selection and acquisition.

9. Lessons Learned

9.1 Software

This project was excellent experience in programming microcontrollers. The hours spent writing and debugging code has built a solid foundation for a career field that makes use of these incredibly useful devices. Software is very versatile but also very sensitive to every detail. Even with the proper flow charts and variable connections, mistakes could occur and easily cause malfunction of the system. Thus, it was important to program in steps that built towards larger system and also have debugging stages so that essential parts of the program can be accessed with ease.

9.2 PCB Design

The first lesson learned in PCB design was that it is a much more complicated process than it seems. The second lesson was to have a solid and complete schematic to work from. This was an important lesson, as changing the schematic added much more work once PCB design as underway than it would have if the schematic was complete from the beginning.

The third lesson was to be flexible with trace routing, and not to get attached to the current routing. Once initial component placement was completed, the trace routing began. After this was complete, it turned out that some components needed to be added, moved, or changed. Rather than restating with no traces, we worked to preserve what we had, which ended up overcomplicating the process further. Once the traces were removed, the re-routing process went smoother.

Designing an RF/Microwave range PCB introduced the team to the concept of designing PCB traces in such a way as to facilitate a 50 Ohm impedance path. We ended up using the grounded coplanar waveguide method, as it worked well for our purposes. This concept was new for most of us, and the experience was new for all of us.

9.3 PCB Assembly

Soldering such tiny pieces was a new experience for the team. Indeed, soldering a PCB in general was a new experience. The skill gained from dispensing just the right amount of solder paste, positioning the component carefully and precisely, then IR-soldering station properly, and inspecting the work will likely be useful as electrical engineers.

9.4 Teamwork

The importance of communication, clearly assigned and defined tasks, mutual respect, and adherence to deadlines were the underlying themes for this project. As practiced as the team was at these concepts coming into the project, we are certainly more familiar with them completing the project.

10. References

Faculty Supervisor: Dr. Jens-Peter Kaps

Sadiku, Matthew N. O. Elements of Electromagnetics. Oxford University Press, 2015.

Jiménez Manuel, et al. Introduction to Embedded Systems Using Microcontrollers and the MSP430. Springer New York, 2014.

Montrose, Mark I. Printed Circuit Board Design Techniques for EMC Compliance: a Handbook for Designers. IEEE Press, 2000.

C. K. Alexander and M. N. O. Sadiku, Fundamentals of Electric Circuits, 5th ed. New York, NY: McGraw-Hill, 2013.

Mantaro,"Impedance Calculators," mantaro.com. [Online], Available: http://mantaro.com/resources/impedance-calculator.htm. [Accessed Nov. 15, 2018].

A. S. Sedra and K. C. Smith, Microelectronic Circuits, 7th ed. New York; Oxford: Oxford University Press, 2015.

RF Micro Devices Inc, NLB-300 Datasheet (DS131015), Greensboro, NC, 2013.

W. Stallings, Data and Computer Communications, 10th ed. Boston: Pearson, 2014.

Analog Devices Inc., ADL5906 Datasheet Rev. A, Norwood, MA, 2013.

Chemandy Electronics, "Coplanar Waveguide with Ground Characteristic Impedance Calculator," chemandy.com. [Online], Available: https://chemandy.com/calculators/coplanar-waveguide-with-ground-calculator.htm . [Accessed Jan. 8, 2019].

11. Appendices

11.1 Appendix A: Proposal

Recording RF Detector for Shielding Effectiveness Testing

Proposal for Senior Design Project
Fall 2018 – Spring 2019

Team Members:

Kevin Riley – Project Manager
Shahed Afrad
Steve Kim
David Phelps

Proposal Submitted: October 9, 2018

A 1. Table of Contents

A 2.Executive Summary

In this age of high tech machineries and complex circuitries, slightest disturbance within a system can have huge impact on the proper functionality. One such disturbance is electromagnetic interference caused by Radio Frequency, RF, environment. To mitigate and prevent outside influence penetrating an enclosed system, shielding material is provided, and before implementation of the shield, it goes through a vital process of electromagnetic susceptibility testing.

The RF exposure in the environment is unpredictable, and to fully compensate for the wide range of RF, Shielding Effectiveness, SE, testing is one of the options for testing electromagnetic susceptibility. The shield enclosure is placed in stirred chamber that sweeps typically from 100kHz to 10GHz, and the current method utilizes a strategic placement of antenna inside the enclosure which is physically wired to the outside analysis unit. The process is time consuming and labor intensive due to the nature of physical altercation of the shield. Also, the process might compromise the accuracy of the testing.

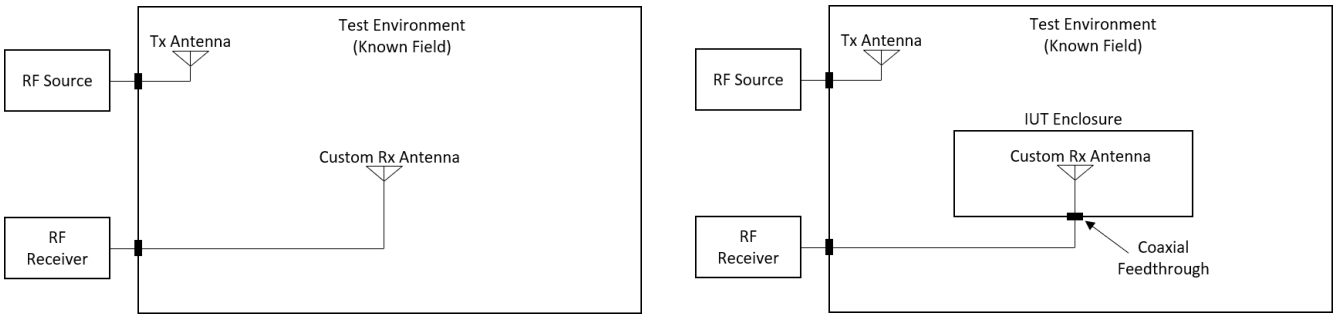
We shall develop two devices that will forgo the process of drilling hole on the shielding for the antenna to be placed and connected. One device shall be a battery powered RF detector unit with antenna attached, which will record incoming RF inside the enclose, and the other device shall be a source monitor unit, which will be synced to the analysis unit to record the RF sweep information. With these two devices, the shield does not have to be modified, which is a preferred way for the owners of the item under test, and also, time and labor required for the current method, which can take hours of preparation and designing, can be saved. The success of our devices will prove the possibility of noninvasive approach to the testing which can be further developed in the future.

To succeed, we will need a thorough understanding of the current procedure of SE testing and the modification that we will be making. The circuitry components, especially the ones concerning RF carrying and processing modules, as well as printed circuit board, PCB, design will be researched extensively, and since our devices shall have multiple components and stages, thorough testing of steps shall be implemented to acquire the optimal accuracy of the recording. Furthermore, power management will be an important factor since battery shall run for about a span of eight hours, and we shall develop robust and optimized devices.

A 3. Problem Statement

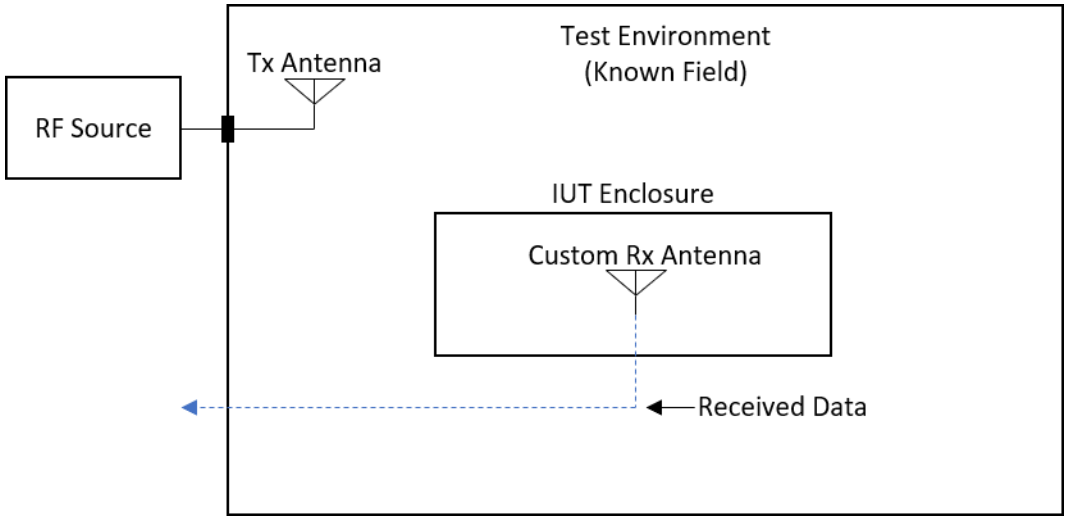
Electromagnetic susceptibility testing determines if an Item Under Test (IUT) will function properly when exposed to the Radio Frequency (RF) environment it will be subjected to in the field. Items tested range from general support equipment to ordnance. It includes testing if the RF will cause interference in IUT circuitry or if sufficient RF energy can couple into Electrically Initiated Devices (EIDs) to cause them to detonate. The latter testing is referred to as Hazard of Electromagnetic Radiation to Ordnance (HERO) testing, and is critical for safety. The RF environments that IUTs are required to be exposed to during testing often include high electric field strengths that can be difficult to generate. One method of reducing this burden is through Shielding Effectiveness (SE) testing. The SE of an enclosure is the ratio of the RF power to which it is exposed, to the RF power measured inside. This value can then be used to determine the maximum field the internal components will be exposed to at the required environment. The internal components can then be exposed to this reduced field level without their enclosure for an equivalent test.

SE is currently measured by constructing a custom antenna that fits within the IUT enclosure. The antenna is connected to a receiver via coaxial cable and is exposed to a known RF field to characterize its response. The antenna is then placed inside the empty IUT enclosure and the enclosure is exposed to a known field while the antenna measures the RF power within. To connect the antenna to the receiver, a coaxial feed-through must be installed in IUT enclosure. This involves drilling a hole through the enclosure, and ensuring this modification does not compromise the SE is labor intensive and time consuming. Additionally, the owner of the IUT often prefers as few modifications to their item as possible. A method of measuring the RF power within an unmodified enclosure is needed.



A 4. Approach

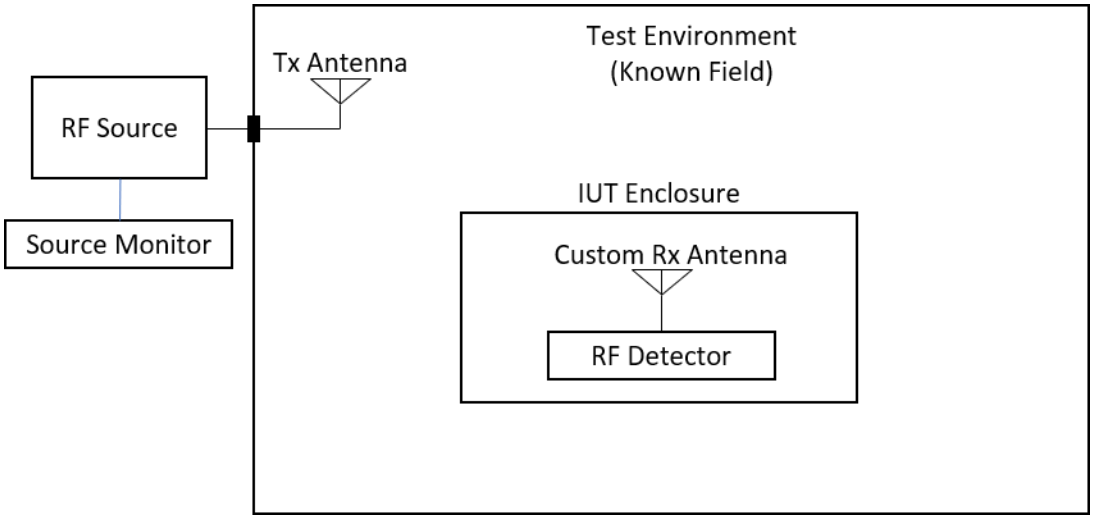
A 4.1 Concept



To mitigate the need to route a coaxial cable through the IUT enclosure, an RF receiver will be built to be placed within the enclosure. Possible methods of transmitting the received data in real-time include wireless RF transmission, sonic transmission, and magnetic transmission. An RF channel is not feasible because the shielding provided by the IUT enclosure would have a significant impact on the channel loss-budget, the RF power transmitted by the receiver would likely drown out the field being measured, and the test environment would likely interfere with the data receiver. A sonic data channel would be high risk, as the audio attenuation of the IUT enclosures cannot be known, there is often broadband ambient sound in the test facility, and the data receiver would need sufficient RF shielding to operate properly in the test environment. A fully magnetic channel, like a pulse encoded magnetic field, is high risk as the permeability of the IUT enclosures cannot be known and the data receiver would need sufficient RF shielding to operate in the test environment. The challenges of real-time data transmission can be overcome by instead recording the RF received by the measurement antenna and retrieving the data after the testing is complete.

A 4.2 Requirements

To ensure the receiver fits within IUTs, the maximum dimensions shall be 6” x 6” x 3”. The receiver shall have an SMA connector to attach to the antenna. Since external power will be unavailable, the device shall be battery powered with a minimum battery life of 8 hours. The data gathered by the receiver will be stored internally during the test and retrieved post-test. Due to the cost and complexity of microwave frequency discrimination, the receiver will only measure the incident RF power and the time at which each measurement occurred, and will henceforth be referred to as the detector. A second device, referred to as the source monitor, will be built to record the time that each RF test frequency was transmitted. The combination of these two data sets provides the information necessary for the test.



The SE testing this device is intended for is conducted from 100 MHz to 10 GHz, requiring a receiver with a minimum detectable power of -60 dBm and a dynamic range of 80 dB. The equipment currently used for this testing exceeds these requirements, having a frequency range of 10 kHz to 18 GHz, a minimum detectable power of less than -80 dBm and a dynamic range of greater than 110 dB. However, due to long lead times of many RF components rated for 10 GHz and the short timeline of this project, the desired frequency range of operation was reduced by the end user to 100 MHz to 6 GHz. This allows the use of more readily available components made for the communications industry. The scope of the project is to prove the modified testing concept, being able to measure received power at microwave frequencies by

post processing recorded data, rather than relying on real-time measurements. Similarly, the end user relaxed sensitivity and dynamic range requirements, to a minimum detectable power of -30 dBm and a dynamic range of 30 dB. The accuracy of the RF power measurement should be within $\pm$ 2 dB, and the detector input impedance should be as close to 50 Ohms as possible. The detector should meet the relaxed requirements, but since the RF frontend will be redesigned after the delivery of this proof of concept device, these are not critical requirements.

During SE testing, the RF environment is swept linearly at a maximum rate of 230 MHz per second, this is based on a 70 second sweep from 2 GHz to 18 GHz, which is the fastest frequency sweep performed. The desired frequency response resolution of the device is at least one sample per MHz. Thus, the detector shall have a sample rate of at least 230 samples per second. The SE testing can consist of up to 700 frequency sweeps from 100 MHz to 10 GHz. This is a 9900 MHz range (10 GHz – 100 MHz) yielding 9900 samples per sweep, the detector shall have data storage for 700 sweeps at 9900 samples per sweep or 6.93 million samples, and the storage amount will be increased to accommodate any sample rate above the minimum.

A 4.3 High-level Implementation

A Commercial Off The Shelf (COTS) RF power sensing Integrated Circuit (IC) will be used to convert the RF signal to a DC signal proportional to the received power. To increase the sensitivity, an RF gain circuit will be used to amplify the RF signal fed to the detector. The gain of the amplifier will be variable to increase the dynamic range. Depending of the profile of the power sensor IC output, a variable DC gain section may be added to further increase the dynamic range. This DC signal will be digitized by an Analog to Digital Converter (ADC). The resolution of the RF received power sample is a function of the ADC resolution, the dynamic range of the RF detector IC, and the resolution of the variable gain stages. These yet unknown parameters prevent the direct calculation of the required ADC resolution. However, due to the modest sample rate, a 16-bit ADC should be a practical option despite sample rate limitations, when compared with the faster lower resolution options. Each digitized sample, along with the gain settings, and the time of the sample will be stored in memory.

The second device, that interfaces with the RF source, records the start time of each frequency sweep via the sync pulse from the source. The source controller records the parameters of each sweep (the duration and frequency range). Each sample from the detector is time stamped, so its temporal location relative to the sync pulse from the RF source is known. Since the rate of change of the frequency is constant during the sweep, and the start frequency is known, the time relative to the sync pulse directly correlates to the frequency that was being transmitted. The source monitor shall be able to record the time of occurrence of 700 pulses. It shall have a USB interface for data transfer to the test computer, configuration via the test computer, and as a power source.

The two devices shall interface with each other, via a microcontroller interface (SPI, I^2C, etc.), before and after each test. Prior to testing this interface will be used to charge the receiver and synchronize the clocks used for time stamps, as well as setting a pretest standby delay. The standby delay will keep the receiver in a low power state for a predetermined amount of time to conserve battery life while it is being installed in the IUT. After the test, the receiver will be removed from the IUT and reconnected to the source monitor. The drift between the two RTCs will measured to ensure the data gathered is valid. The data collected by the receiver will be passed through the source monitor to the test computer via the source monitor USB interface. The source monitor will have an LCD display to convey the state of the battery in the receiver while charging, the amount of standby delay remaining after disconnection, and the sync pulse count during testing. The sync pulse count will be used to verify that the source monitor has captured the expected number of sweeps during testing.

A 5. System Design

A 5.1 Functional Decomposition of Detector Unit

A 5.1.A Level-0 Top-Level Functions

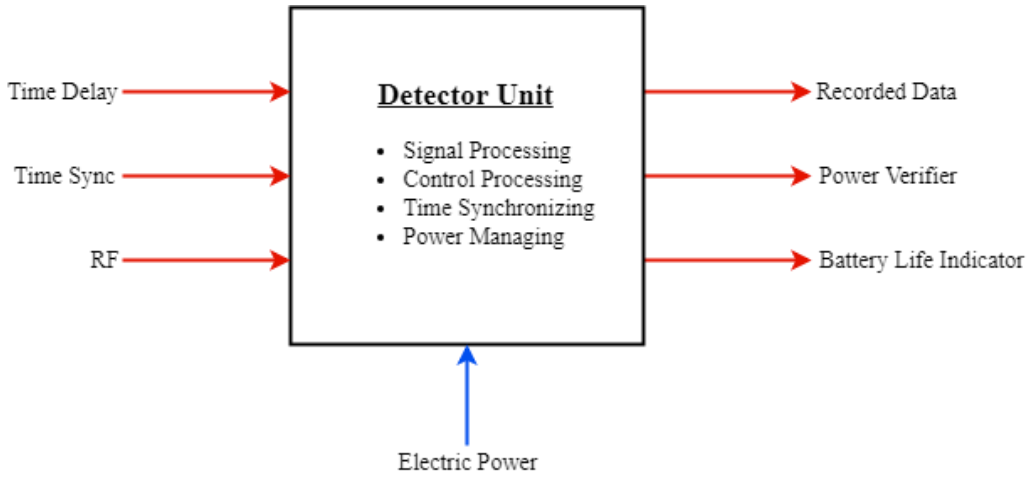


Figure 24: Level-0 Top-Level Functions of Detector Unit

A 5.1.B Level-1 Functional Decomposition

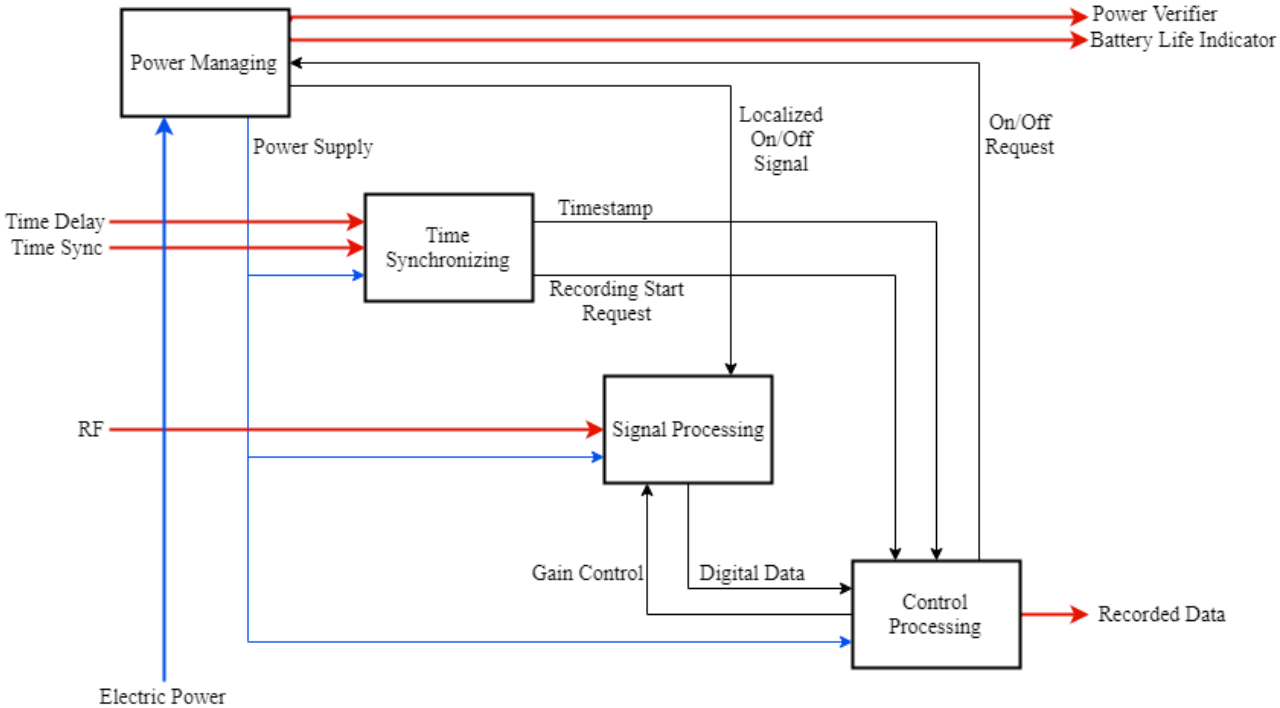


Figure 25: Level-1 Functional Decomposition of Detector Unit

A 5.1.C Level-2 Functional Decompositions

Function: Power Managing

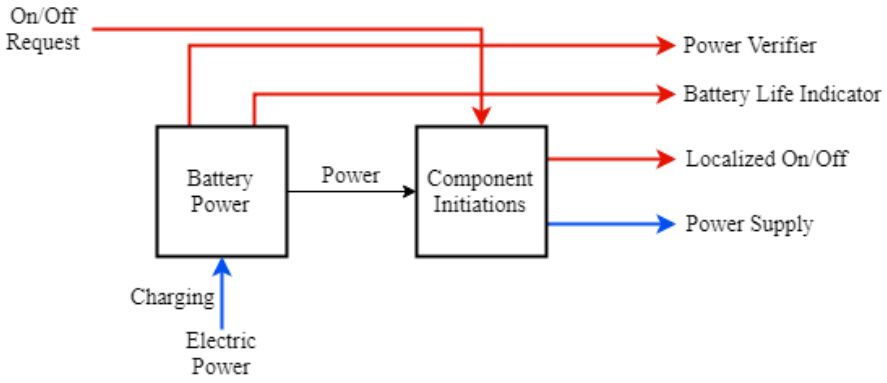


Figure 26:Level-2 Functional Decomposition of Power Managing

Function: Time Synchronizing

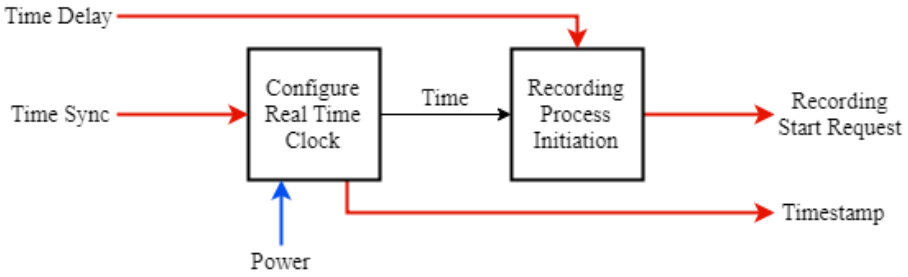


Figure 27: Level-2 Functional Decomposition of Time Synchronizing

Function: Signal Processing

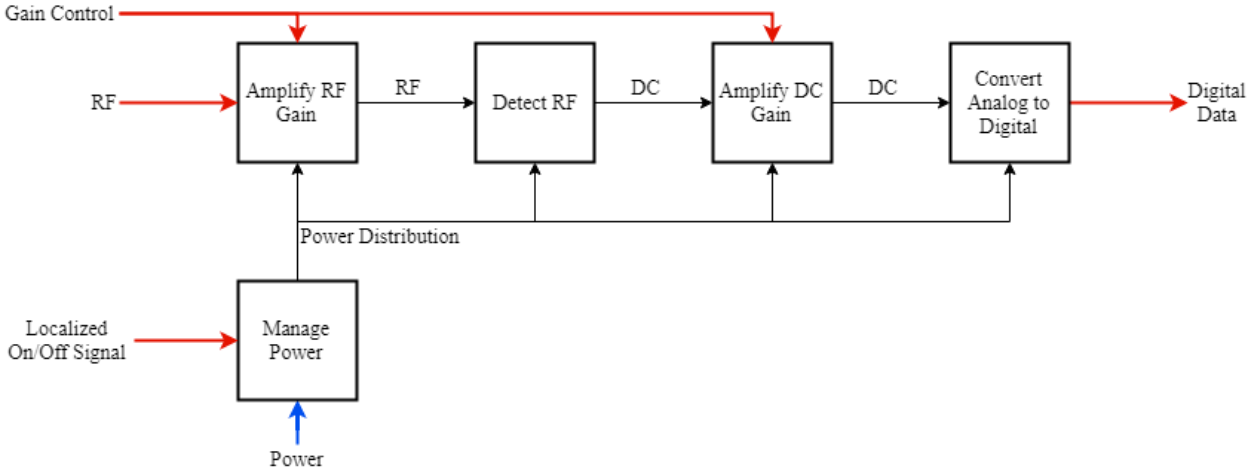


Figure 28: Level-2 Functional Decomposition of Signal Processing

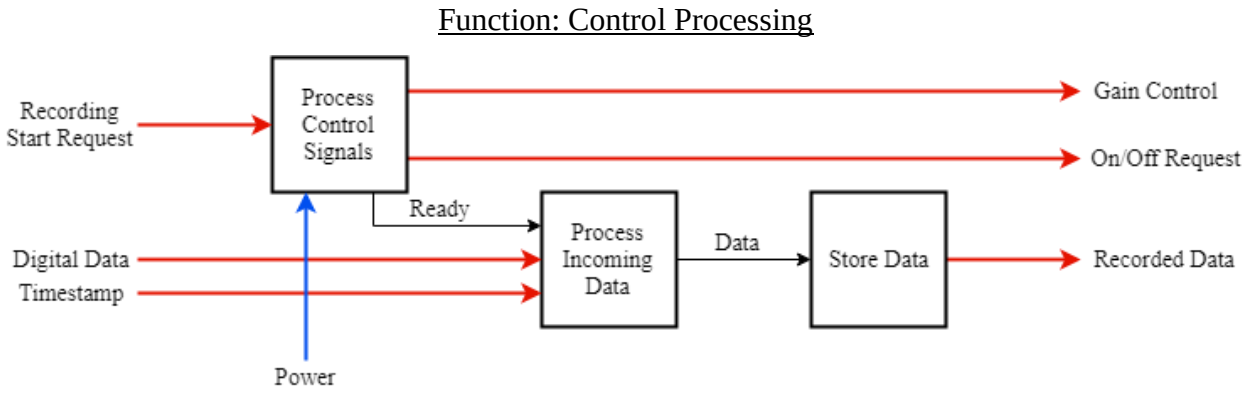


Figure 29: Level-2 Functional Decomposition of Control Processing

A 5.2 Functional Decomposition of Source Monitor Unit

A 5.2.A Level-0: Top-Level Functions

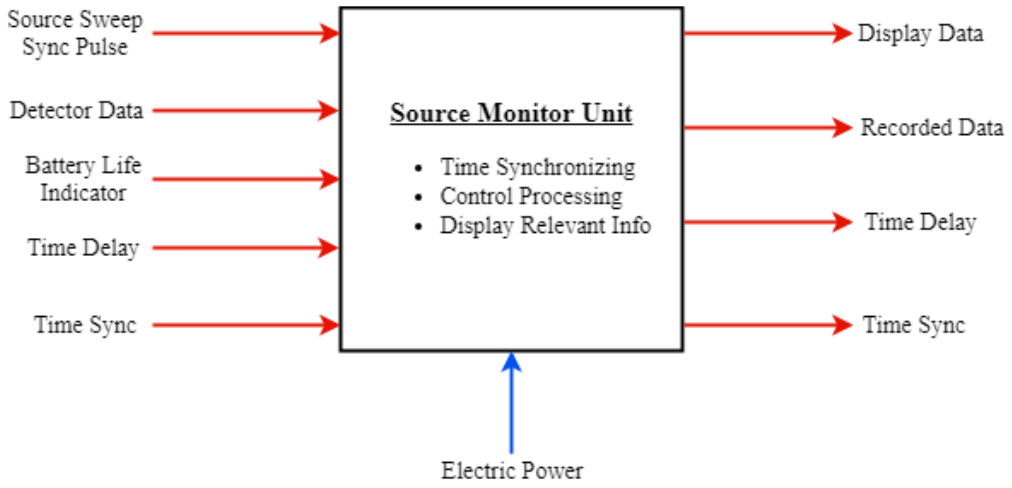


Figure 30: Level-0 Top-Level Functions of Source Monitor Unit

A 5.2.B Level-1 Functional Decomposition

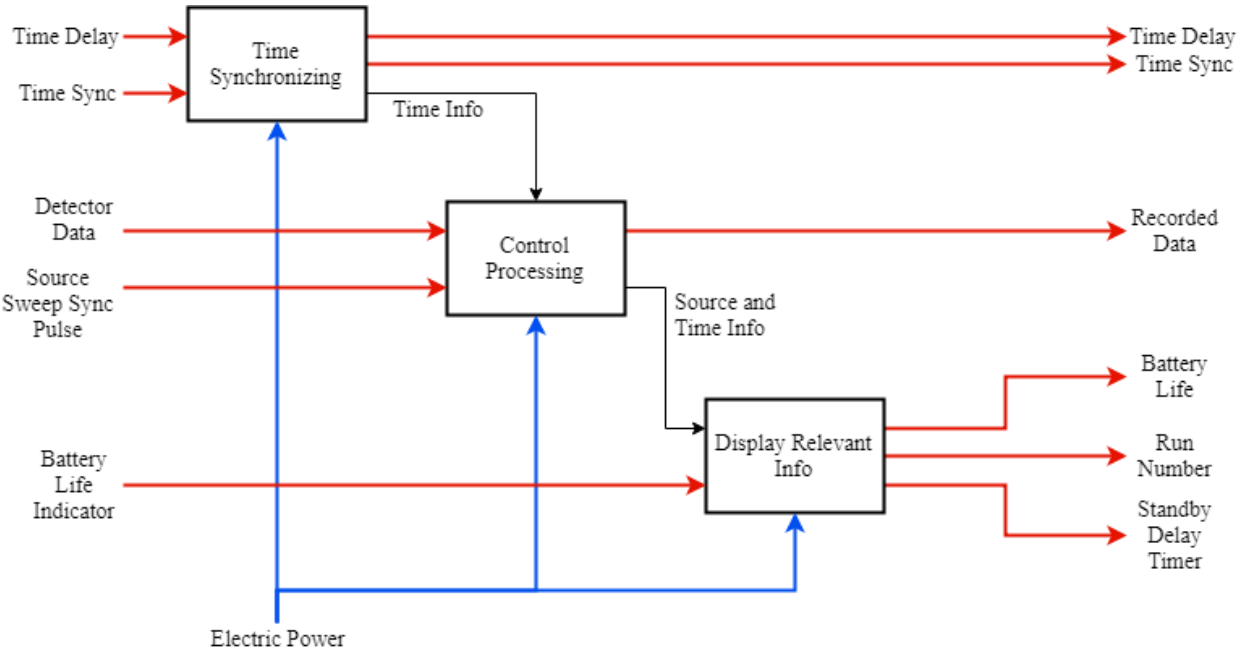


Figure 31: Level-1 Functional Decomposition of Source Monitor Unit

A 5.2.C Level-2 Functional Decompositions

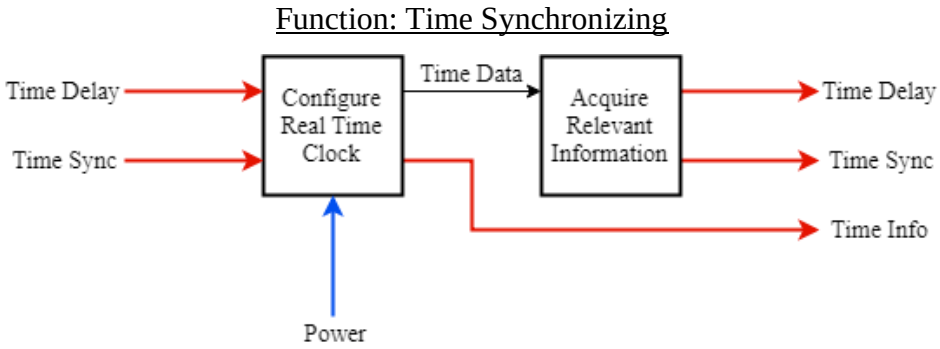


Figure 32Level-2 Functional Decomposition of Time Synchronizing

Function: Control Processing

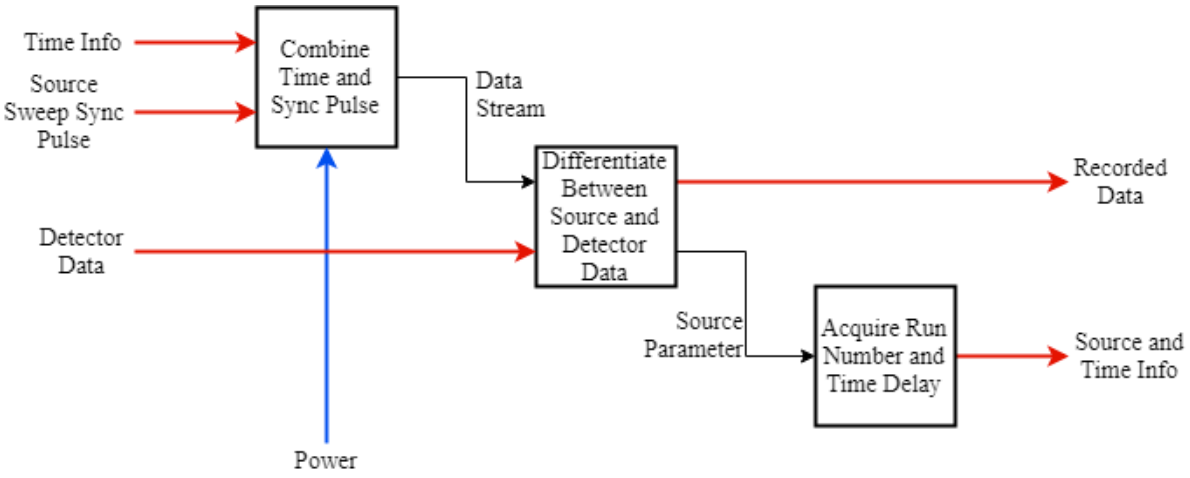


Figure 33Level-2 Functional Decomposition of Control Processing

Function: Display Relevant Info

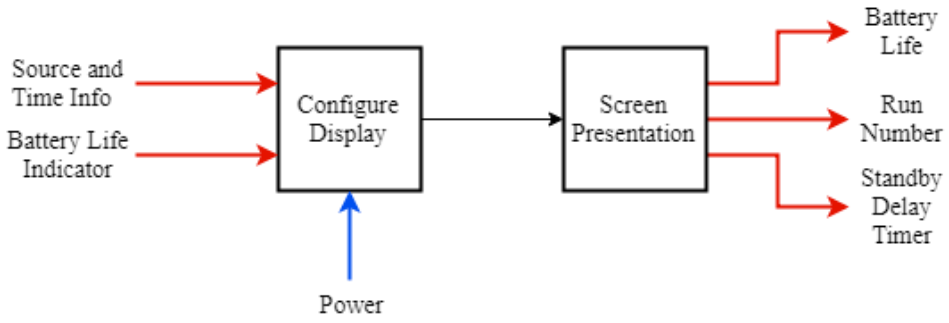


Figure 34Level-2 Functional Decomposition of Display Relevant Information

A 5.3 Architecture of Detector Unit

A 5.3.A Physical Architecture

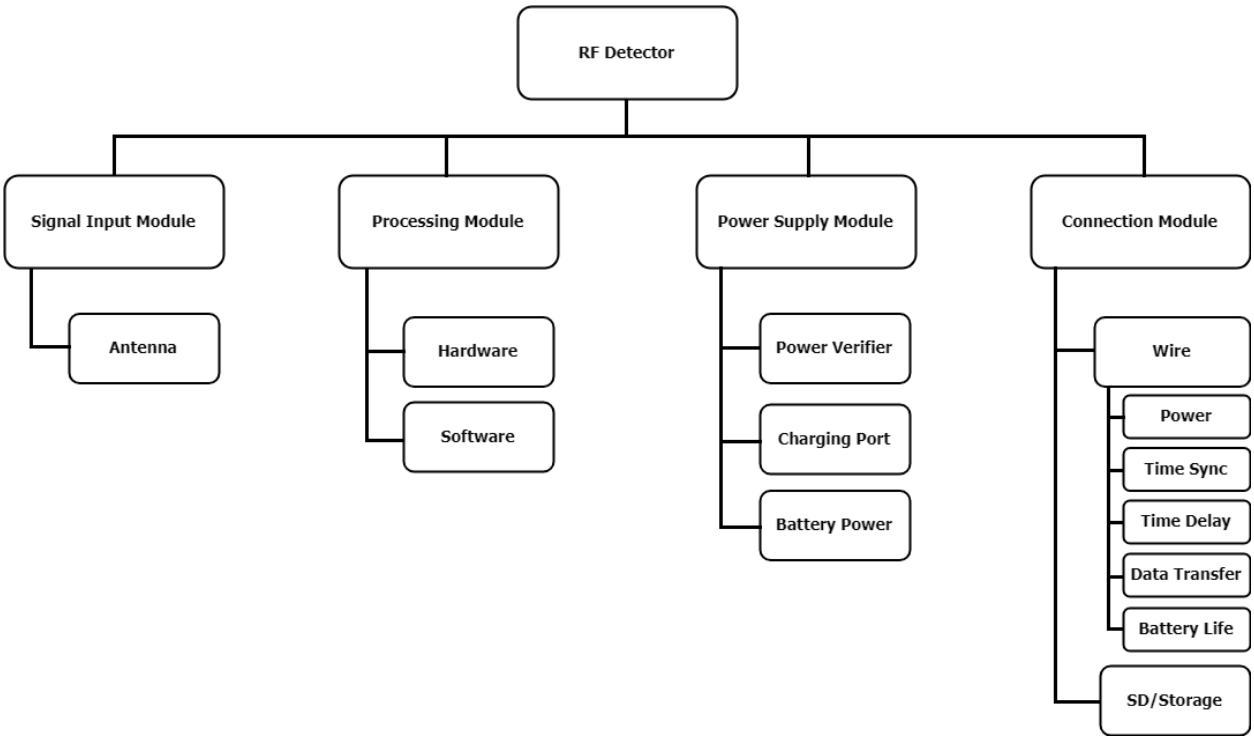
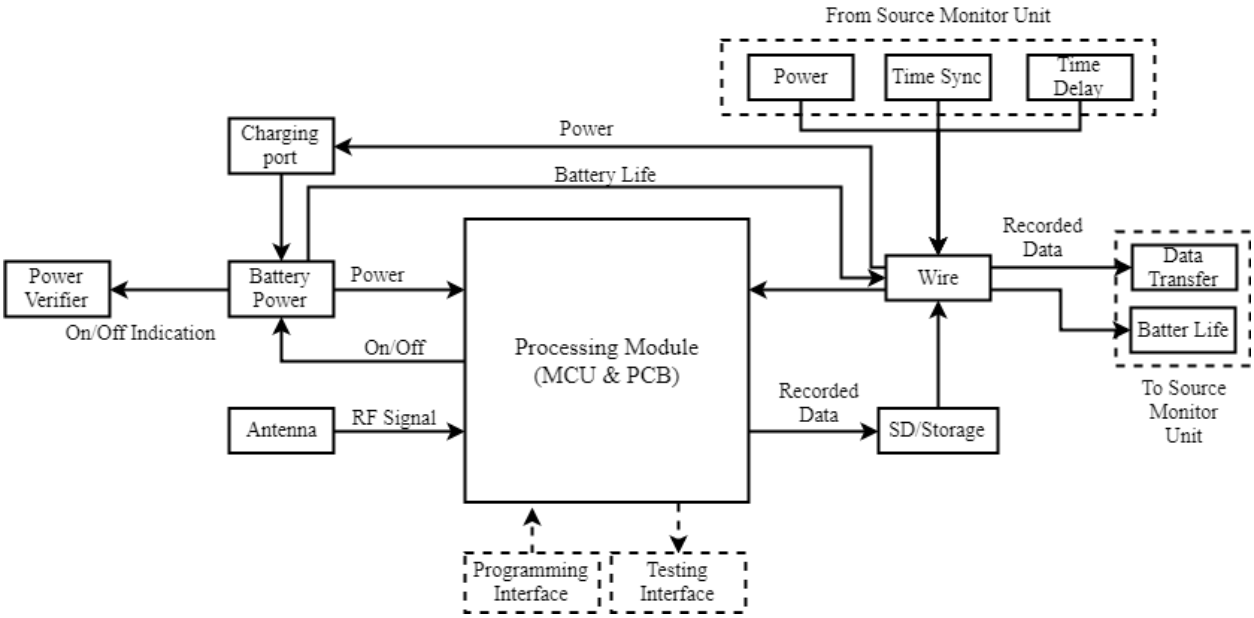


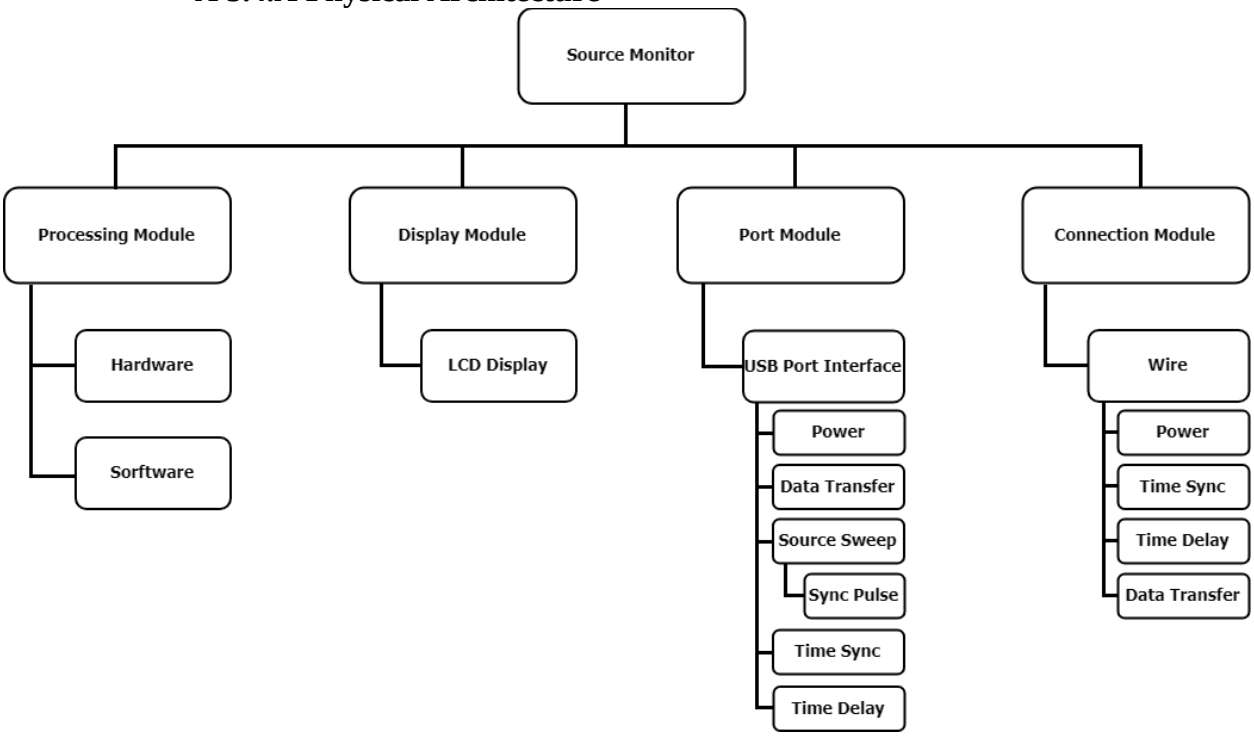
Figure 35: Physical Architecture of Detector Unit

A 5.3.B System Architecture

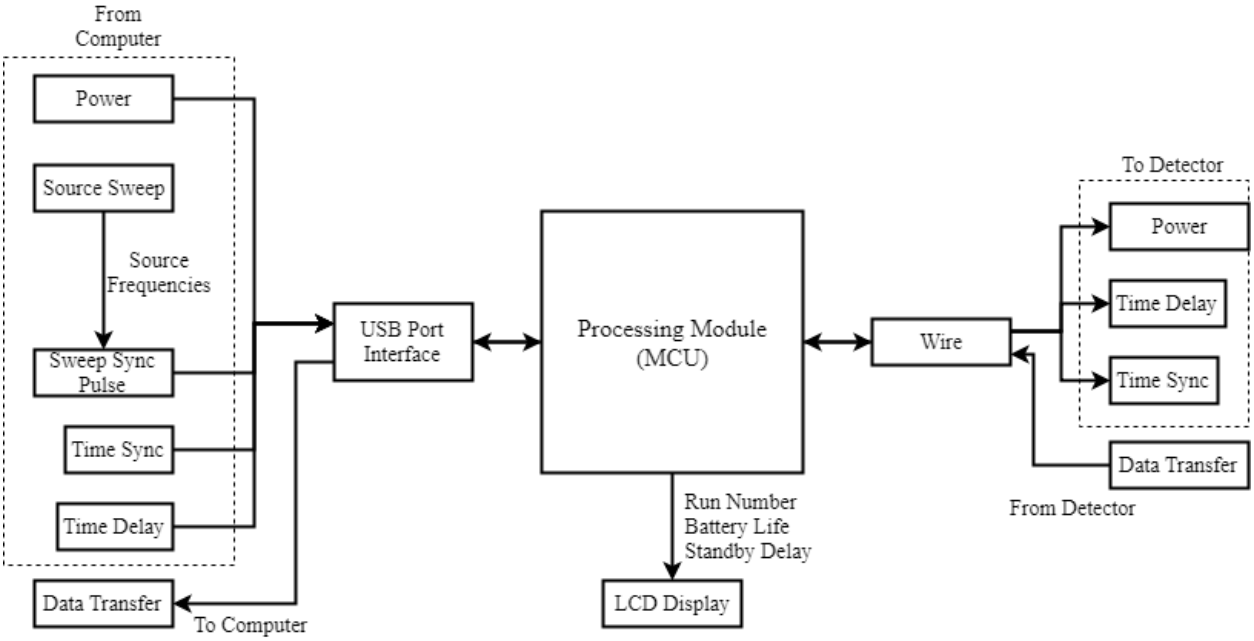


A 5.4 Architecture of Source Monitor Unit

A 5.4.A Physical Architecture



A 5.4.B System Architecture



A 5.5 System Setup

A 5.5.A Pre-Recording Setup

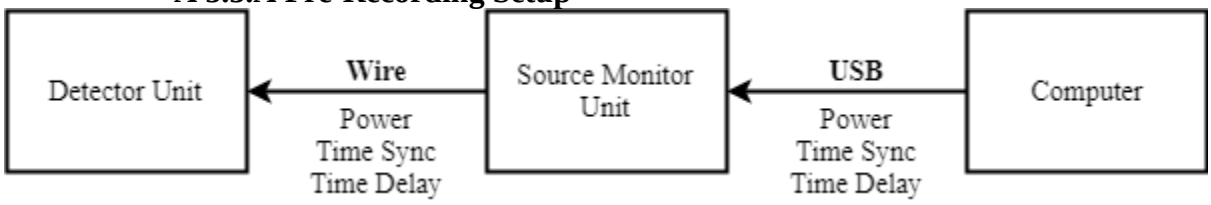


Figure 36: Pre-Recording Setup

5.5.B During Recording Setup

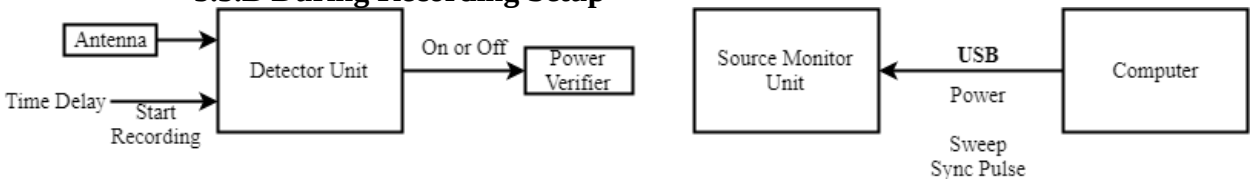


Figure 37: During Recording Setup

A 5.5.A Post-Recording Setup

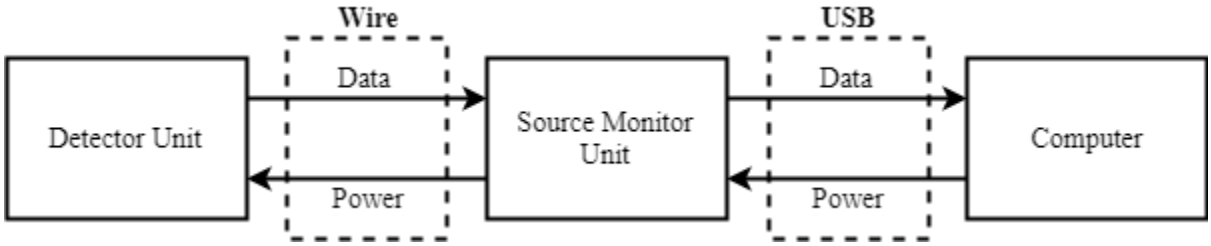


Figure 38: Post-Recording Setup

A 6. Preliminary Experimentation Plan

As is expected of a device made up of many smaller devices integrated together, each component should be tested individually, then tested as a part of a larger system, and finally tested at the highest level, being integrated into the device itself. Due to the nature of the Recording RF Detector for Shielding Effectiveness Testing, the Detector Unit shall operate as intended in an environment filled with RF signals. Often, exposure to RF signals can interfere or even damage electronics. As such, the device should behave the same way in an RF-environment as it does in a controlled environment. The specifics of this type of experimentation will depend on the components used in the system, as well as access to an appropriate RF-environment.

Of the Detector Unit itself, the chief concerns are the testing of minimum detectable power, dynamic range, and frequency response. This can be achieved within one experiment, and will ultimately determine whether or not the device meets the requirements from NSWC Dahlgren. Minimum detectable power will be important, as it will be used to determine the shielding effectiveness of the enclosure-under-test. If the device is not detecting an RF signal at certain frequencies, the shielding will be assumed to be of at least a certain effectiveness. To avoid erroneous conclusions, this data should be tested and confirmed for accuracy. The dynamic range of the device will provide the range over which the data is considered reliable, and should meet or exceed the requirements for the project. The frequency response of the device shall be considered and mapped, to make adjustments to the data in order to compensate for any discrepancies. The experiment that will test for these purposes will be to input known RF signals into the device directly, rather than rely on radiated signals received via antenna. This will provide exact amplitudes and frequencies of input signals to compare with output data.

A third experiment that should be conducted is that of the power consumption and battery life of the device. Given that the Detector Unit is required to operate on battery power for 8 hours between charges, the maximum expected power consumption should be calculated. With this data, a battery will be selected and the battery life verified. Ideally this experiment would be done with the battery connected to the device, but it may likely be the case that the device's peak power consumption occurs only during times of exposure to detectable levels of RF signals, in which case testing for battery life may be difficult to achieve, given the restrictions on RF radiation. In this case, testing the battery individually may be sufficient prior to testing the device in NSWC Dahlgren's RF chamber.

A 7. Preliminary Project Plan

A 7.1 Short List of Tasks for ECE493

We shall finish the blueprint of our device at the end of this semester and finalized the numerical values of the components and will find COTS components according to our specifications. We shall build every block of our system architecture and test functionality of each blocks to check accuracy and shall integrate all components to find where we will make adjustment to meet client's requirements. At the end of ECE492, we shall finish PCB design and integrate all functional blocks on printed circuit board. We shall test our final device at client's facility to get feedback and will modify system functionality if necessary.

A 7.2 Allocation of Responsibilities

Kevin Riley is the project manager. He is the point of contact with client. Kevin shall design the control part of device and responsible for embedded programming of microcontroller. Also, he is responsible for designing output data memory system.

Steve Kim shall research on RF sensor and integration of RF sensor. He will keep track of function interaction between system blocks. Also, he shall implement Analog to Digital Converter (ADC) within the system.

David Phelps is the Assistant Project Manager. He shall design the Radio Frequency Printed Circuit Board (RF PCB). He is responsible for system's power management design. Also, he shall conduct research on PCB technology.

Shahed Afrad shall conduct research on RF Amplifiers and the integration of the RF Amplifier. He is responsible for research on the client-provided, front-end antenna. He shall integrate the RF amplifier within the system. Also, he is responsible for user interface design.

A 8. Potential Problems

A 8.1 Knowledge and Skills to be Learned as a Group

We shall learn embedded system programming as we shall use a microcontroller as out control unit. We shall learn PCB design technology. Also, we shall learn how to integrate HF components without electromagnetic interference. More generally, the group must learn to work together to meet deadlines, rely on each other for certain interlocking subprojects and designs, and be able to integrate individual contributions into a working project. This project will provide opportunities for both technical and teamwork skills to be developed and honed.

A 8.2 Project Risk Analysis

Overall, the RF realm tends to be present its own complicated problems, which may need to be addressed as they arise. RF PCB design will be big challenge, as it has more specific requirements than typical PCB circuits. Another concern is insufficient RF gain, since the device should have a relatively low power minimally detectable signal. Lack of high frequency sensitivity of the RF sensor could be a problem. The components of the device itself may need to be shielded to prevent RF interference or damage. As such, care should be taken to ensure that each individual component is protected from the wide band of RF signals the device will be exposed to, and will indeed have running through the device itself. PCB design and fabrication itself will be a potential problem, as a working RF PCB could take time to achieve.

A 9. References

- Faculty Supervisor: Dr. Jens-Peter Kaps
- Sadiku, Matthew N. O. Elements of Electromagnetics. Oxford University Press, 2015.
- Jiménez Manuel, et al. Introduction to Embedded Systems Using Microcontrollers and the MSP430. Springer New York, 2014.
- Montrose, Mark I. Printed Circuit Board Design Techniques for EMC Compliance: a Handbook for Designers. IEEE Press, 2000.

Recording RF Detector for Shielding Effectiveness Testing

Design Document for Senior Design Project
Fall 2018 – Spring 2019

Team Members:

Kevin Riley – Project Manager
Shahed Afrad
Steve Kim
David Phelps

B 1. Table of Contents

B 2. Short Review

We are in the process of creating a system to detect and record the RF shielding effectiveness of a given enclosure. Our system consists of two main devices, the Detector Unit and the Source Monitor. These devices are first connected, allowing their clocks to synchronize. The testing to be completed involves a series of broadcasted RF signal sweeps over 8 hours. This RF sweep occurs in a test environment in order to characterize the enclosure-under-test. Before beginning testing, the Detector Unit is placed inside the enclosure-under-test, attached to a custom RF antenna within the antenna, and begins detecting and recording incoming data, with a time stamp. The Source Monitor remains connected to the computer controlling the RF signal transmission, and records data on what is being broadcasted to the enclosure and at what time. Following the conclusion of the test, the Detector Unit is retrieved, and the two devices are connected. The devices then share their data, synchronizing detected data from the Detector Unit with that of the Source Monitor. This provides the necessary data to compute the shielding effectiveness of that enclosure for the range of frequencies performed in the test.

B 3. Requirements Specification

To ensure the receiver fits within the enclosures-under-test, the maximum dimensions shall be 6” x 6” x 3”. The receiver shall have an SMA connector to attach to the antenna. Since external power will be unavailable, the device shall be battery powered with a minimum battery life of 8 hours. The data gathered by the receiver will be stored internally during the test and retrieved post-test. Due to the cost and complexity of microwave frequency discrimination, the receiver will only measure the incident RF power and the time at which each measurement occurred, and will henceforth be referred to as the detector. A second device, referred to as the source monitor, will be built to record the time that each RF test frequency was transmitted. The combination of these two data sets provides the information necessary for the test.

The SE testing this device is intended for is conducted from 100 MHz to 10 GHz, requiring a receiver with a minimum detectable power of -60 dBm and a dynamic range of 80 dB. The equipment currently used for this testing exceeds these requirements, having a frequency range of 10 kHz to 18 GHz, a minimum detectable power of less than -80 dBm and a dynamic range of greater than 110 dB. However, due to long lead times of many RF components rated for 10 GHz and the short timeline of this project, the desired frequency range of operation

was reduced by the end user to 100 MHz to 6 GHz. This allows the use of more readily available components made for the communications industry. The scope of the project is to prove the modified testing concept, being able to measure received power at microwave frequencies by post processing recorded data, rather than relying on real-time measurements. Similarly, the end user relaxed sensitivity and dynamic range requirements, to a minimum detectable power of -30 dBm and a dynamic range of 30 dB. The accuracy of the RF power measurement should be within $\pm$ 2 dB, and the detector input impedance should be as close to 50 Ohms as possible. The detector should meet the relaxed requirements, but since the RF frontend will be redesigned after the delivery of this proof of concept device, these are not critical requirements.

During SE testing, the RF environment is swept linearly at a maximum rate of 230 MHz per second, this is based on a 70 second sweep from 2 GHz to 18 GHz, which is the fastest frequency sweep performed. The desired frequency response resolution of the device is at least one sample per MHz. Thus, the detector shall have a sample rate of at least 230 samples per second. The SE testing can consist of up to 700 frequency sweeps from 100 MHz to 10 GHz. This is a 9900 MHz range (10 GHz – 100 MHz) yielding 9900 samples per sweep, the detector shall have data storage for 700 sweeps at 9900 samples per sweep or 6.93 million samples, and the storage amount will be increased to accommodate any sample rate above the minimum.

B 4. System Design/Architecture

B 4.1 Functional Decomposition of Detector Unit

4.1.A Level-0 Top-Level Functions

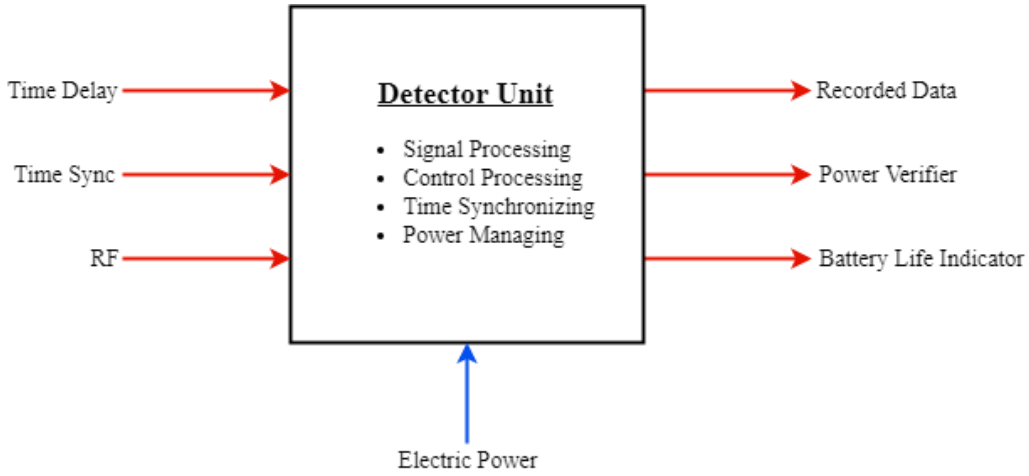


Figure 39: Level-0 Top-Level Functions of Detector Unit

B 4.1.B Level-1 Functional Decomposition

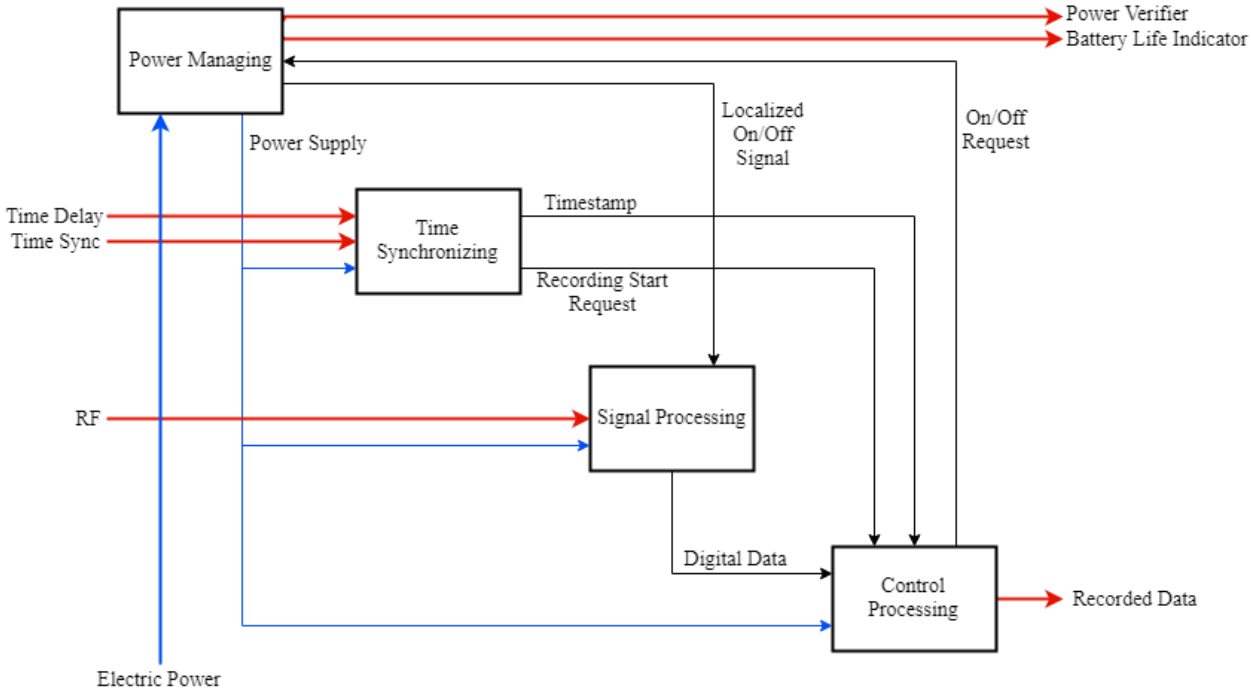


Figure 40: Level-1 Functional Decomposition of Detector Unit

B 4.1.C Level-2 Functional Decompositions

Function: Power Managing

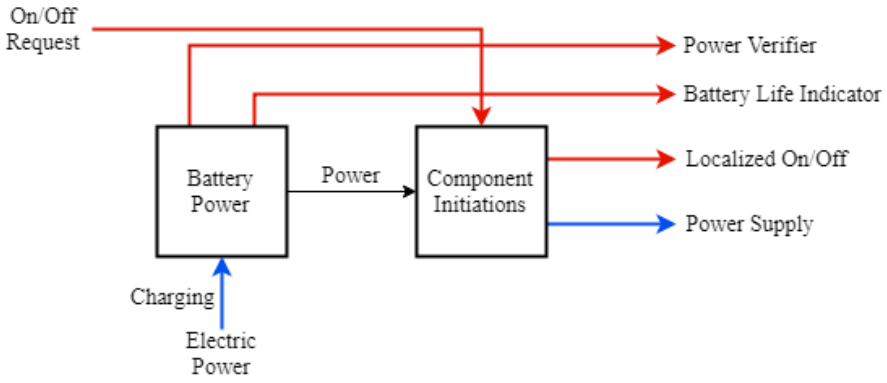


Figure 41: Level-2 Functional Decomposition of Power Managing

Function: Time Synchronizing

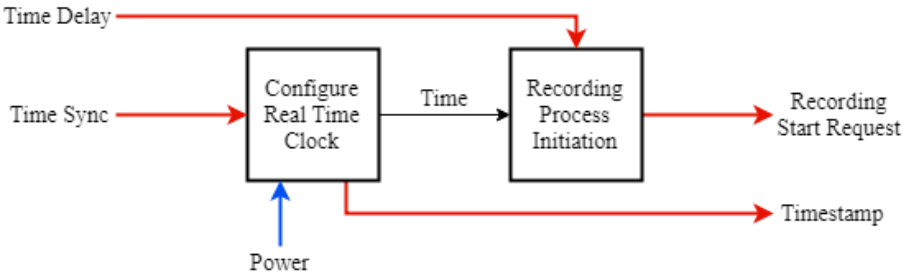


Figure 42: Level-2 Functional Decomposition of Time Synchronizing

Function: Signal Processing

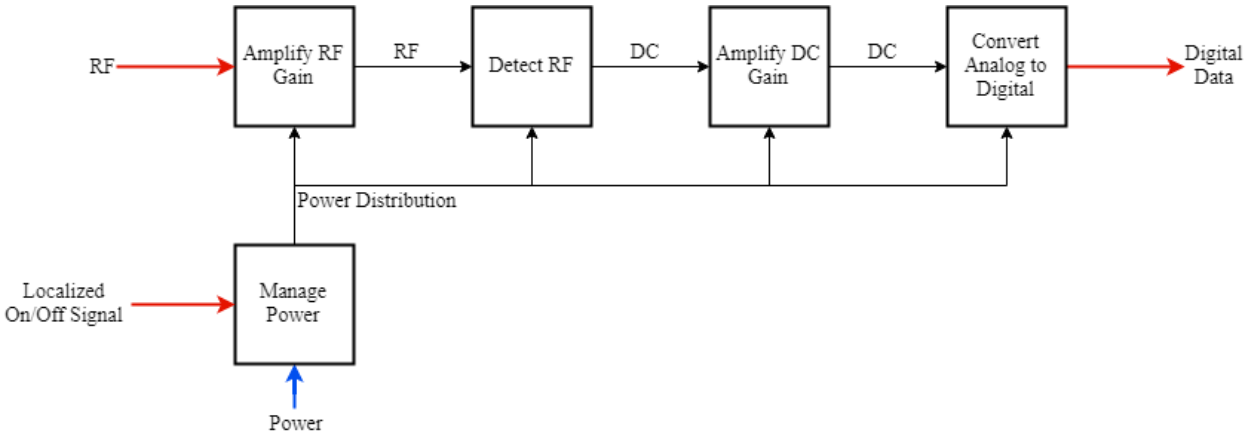


Figure 43: Level-2 Functional Decomposition of Signal Processing

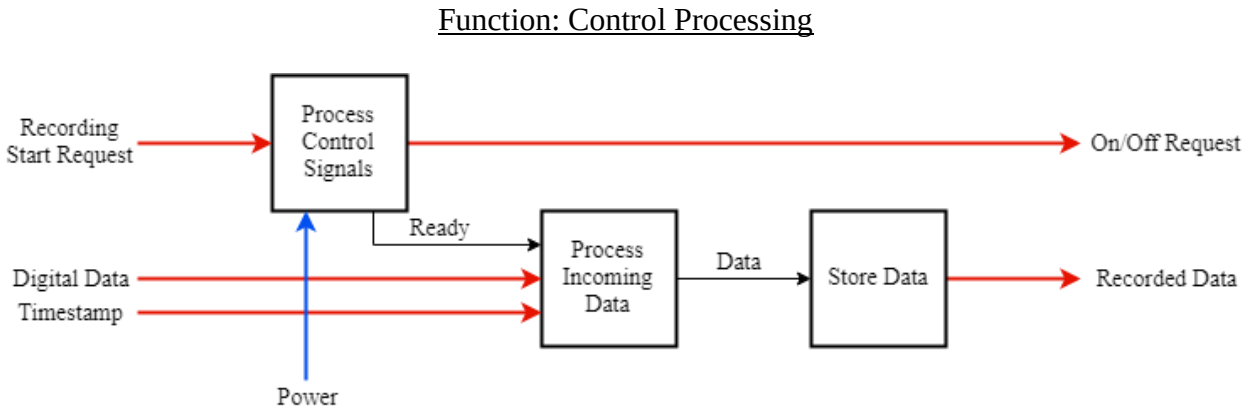


Figure 44: Level-2 Functional Decomposition of Control Processing

B 4.2 Functional Decomposition of Source Monitor Unit

B 4.2.A Level-0: Top-Level Functions

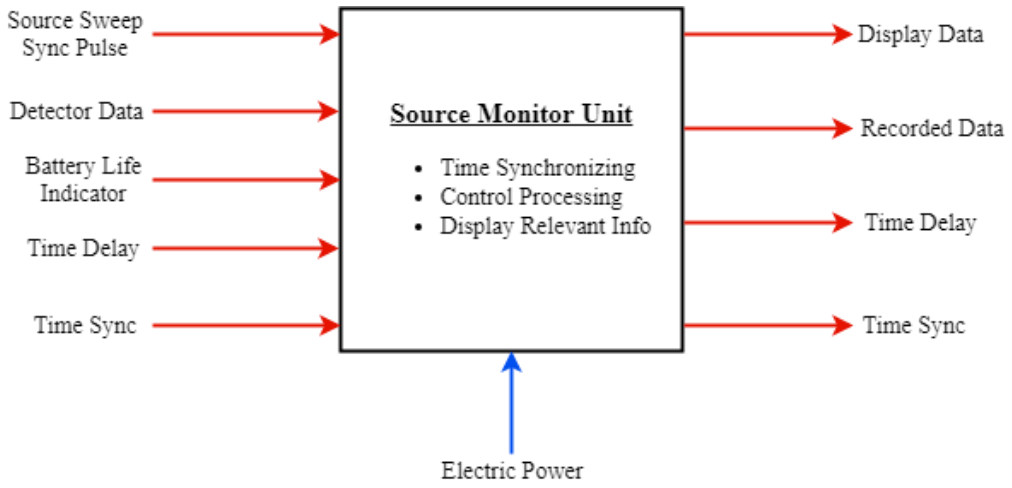


Figure 45: Level-0 Top-Level Functions of Source Monitor Unit

B 4.2.B Level-1 Functional Decomposition

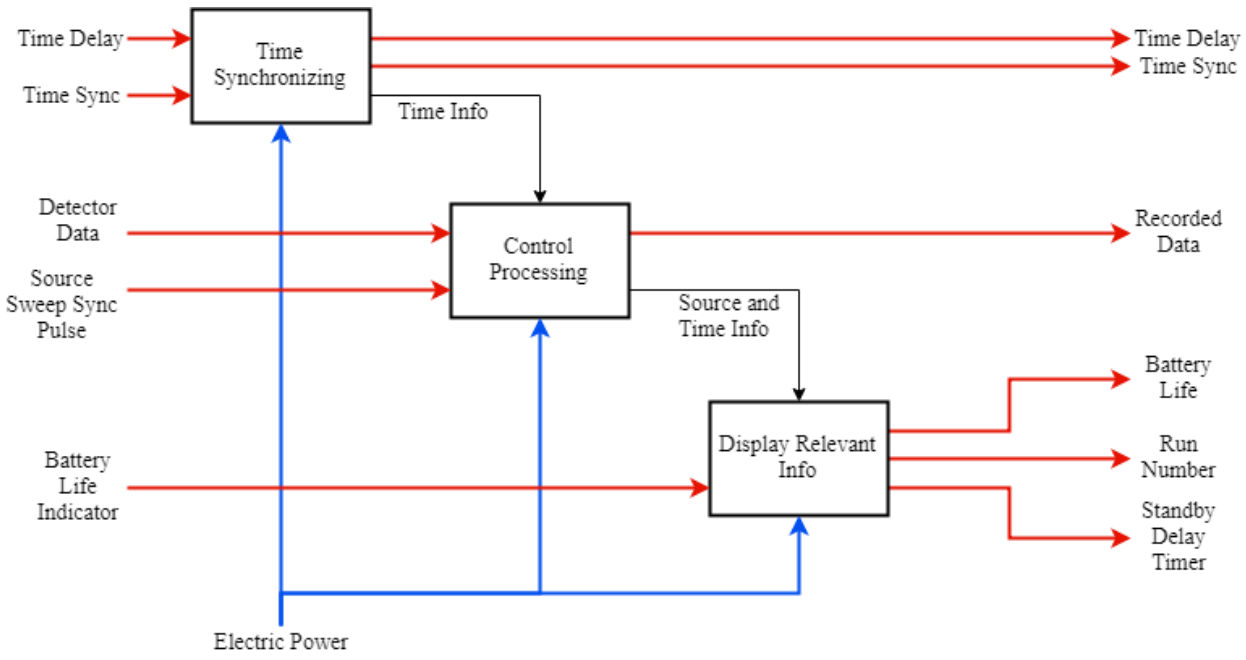


Figure 46: Level-1 Functional Decomposition of Source Monitor Unit

B 4.2.C Level-2 Functional Decompositions

<u>Function: Time Synchronizing</u>

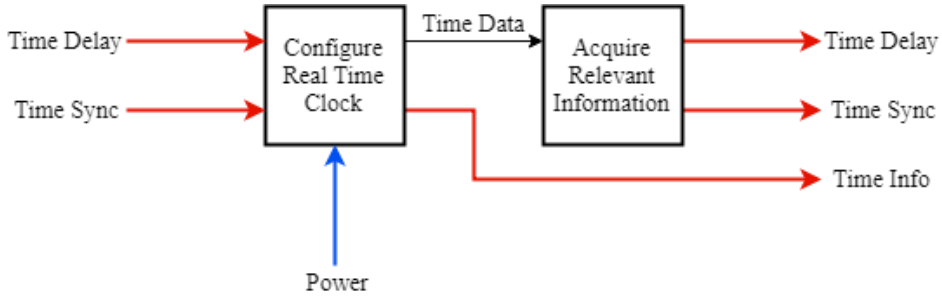


Figure 47: Level-2 Functional Decomposition of Time Synchronizing

Function: Control Processing

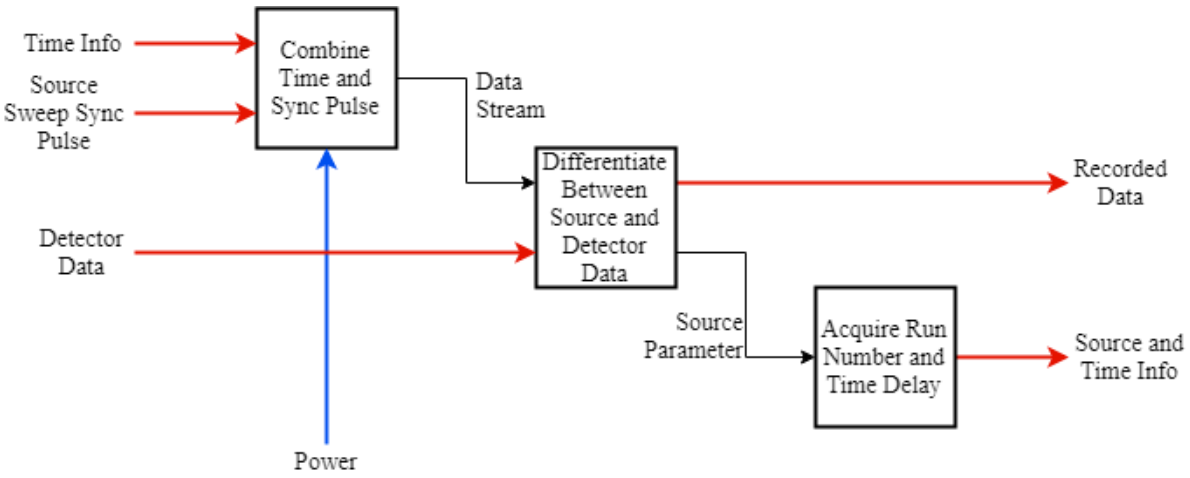


Figure 48: Level-2 Functional Decomposition of Control Processing

Function: Display Relevant Info

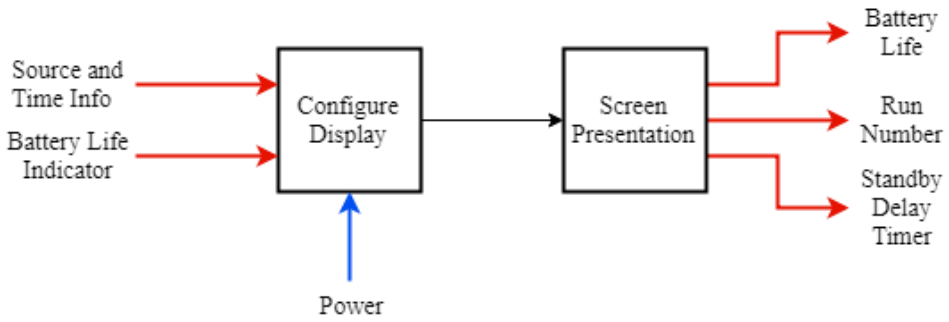


Figure 49: Level-2 Functional Decomposition of Display Relevant Information

B 4.3 Architecture of Detector Unit

B 4.3.A Physical Architecture

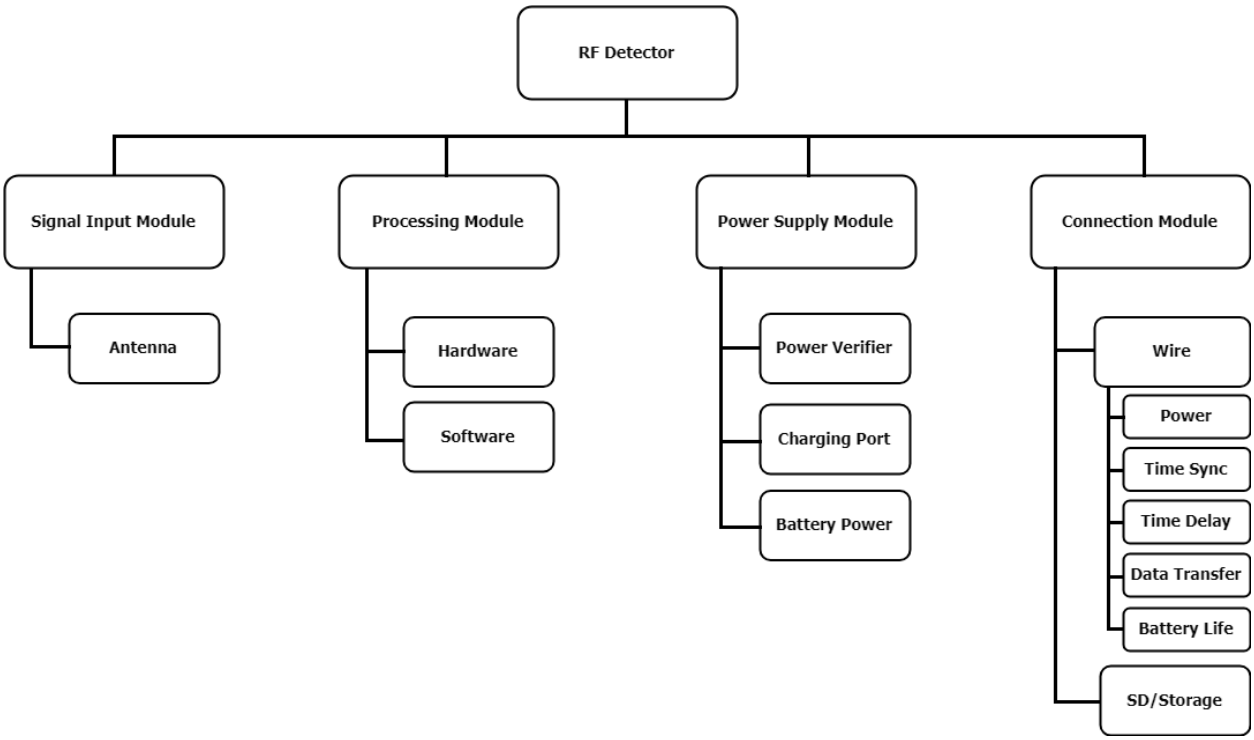
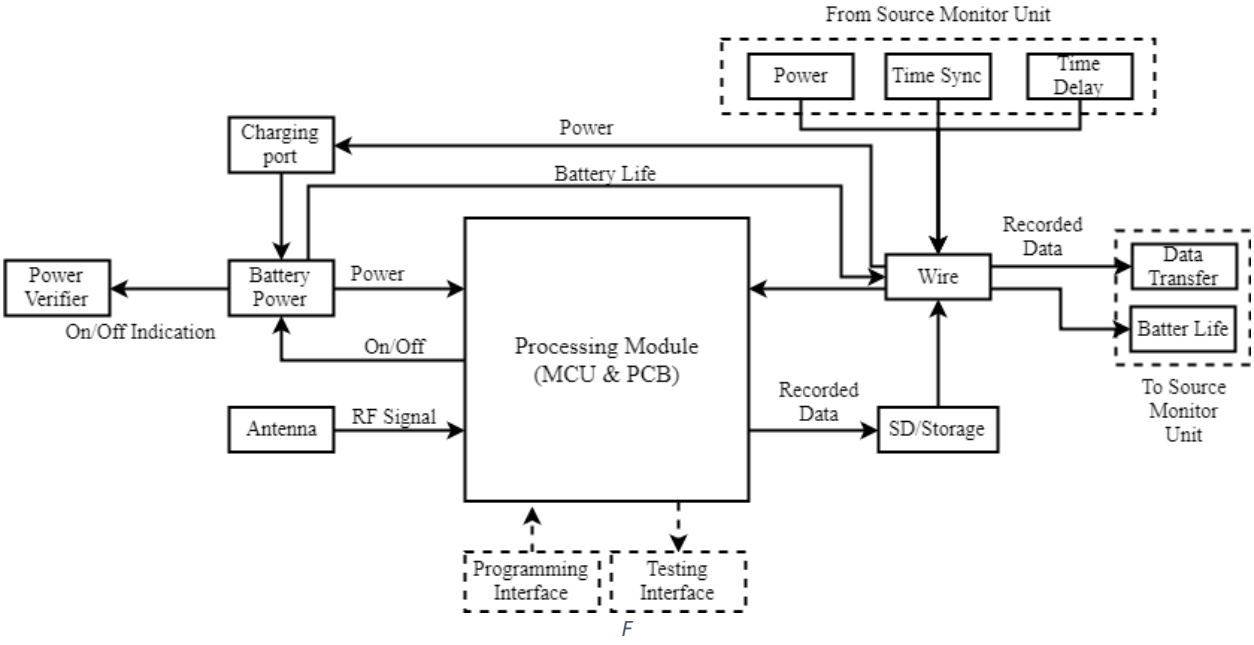


Figure 50: Physical Architecture of Detector Unit

B 4.3.B System Architecture



F

Figure 51: System Architecture of Detector Unit

B 4.4 Architecture of Source Monitor Unit

B 4.4.A Physical Architecture

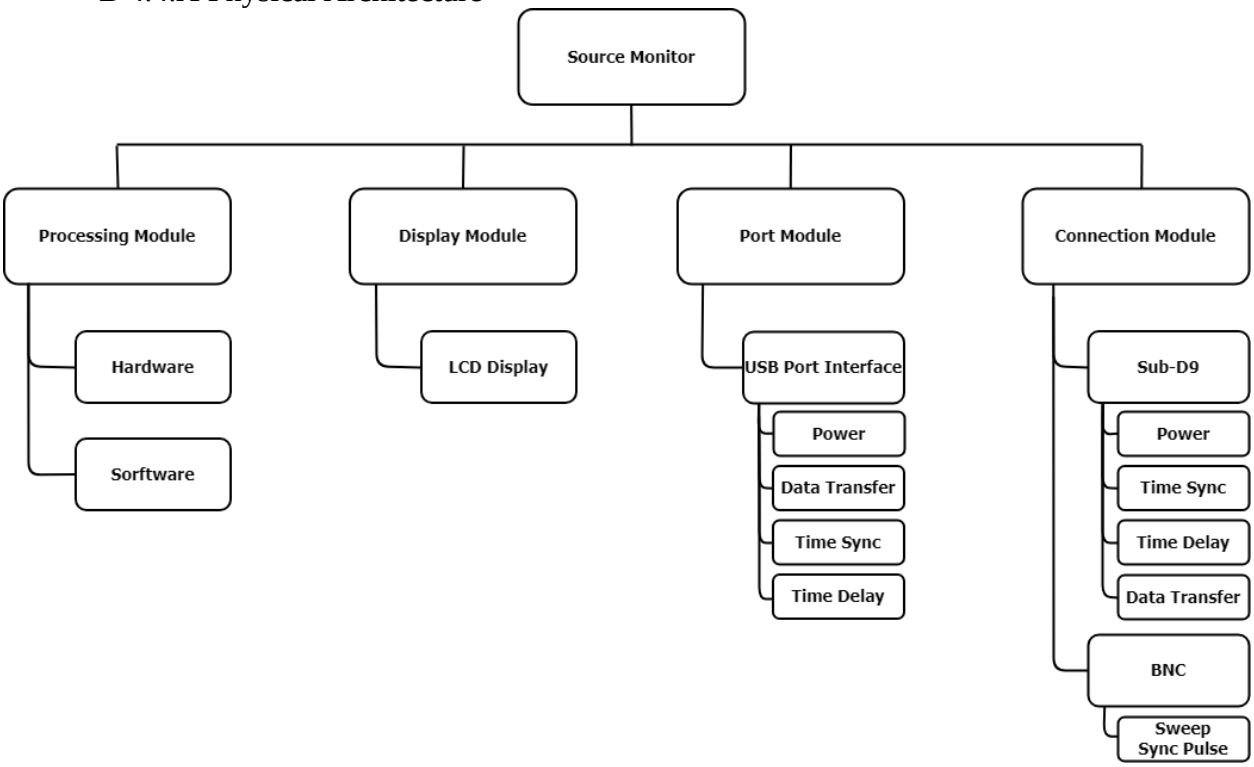


Figure 52: Physical Architecture of Source Monitor Unit

B 4.4.B System Architecture

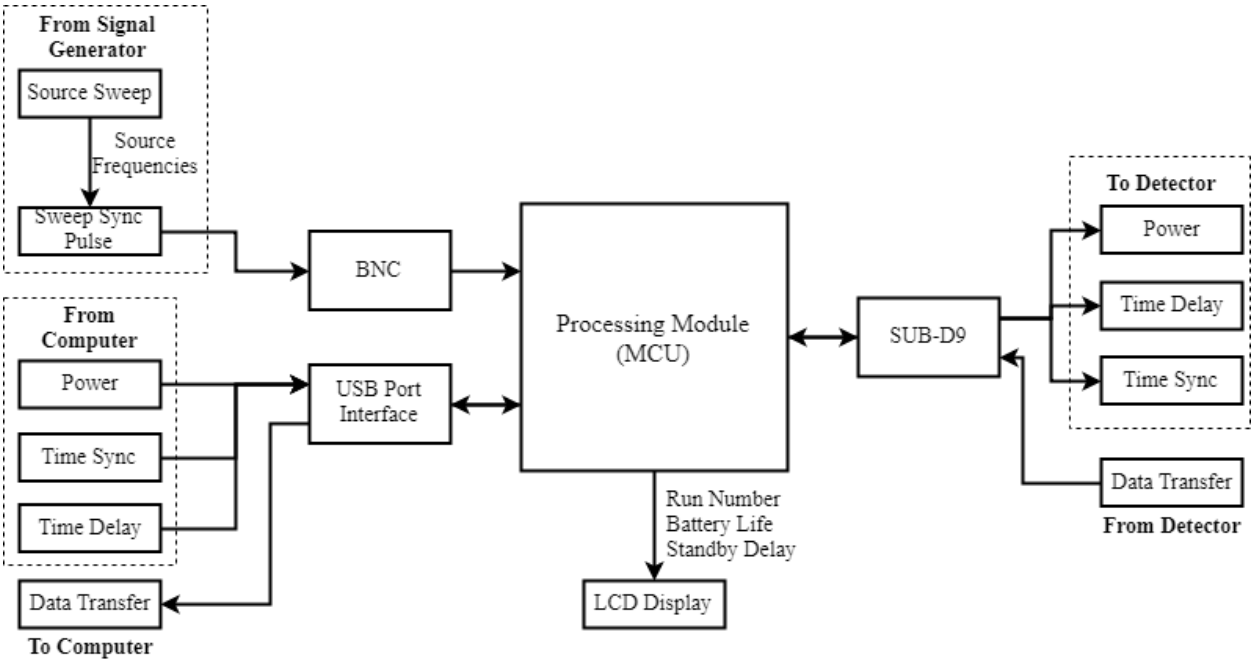


Figure 53: System Architecture of Source Monitor Unit

B 4.5 System Setup

B 4.5.A Pre-Recording Setup

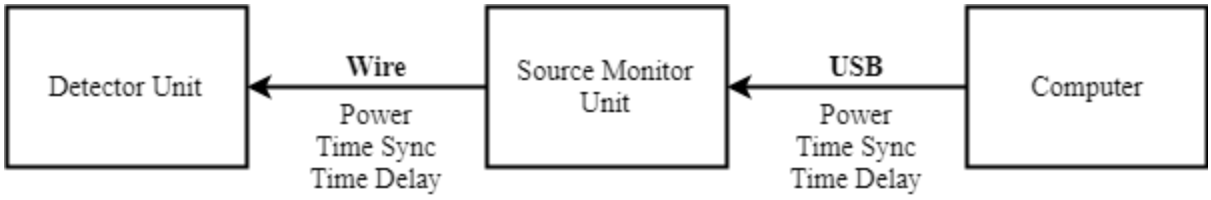


Figure 54: Pre-Recording Setup

B 4.5.B During Recording Setup

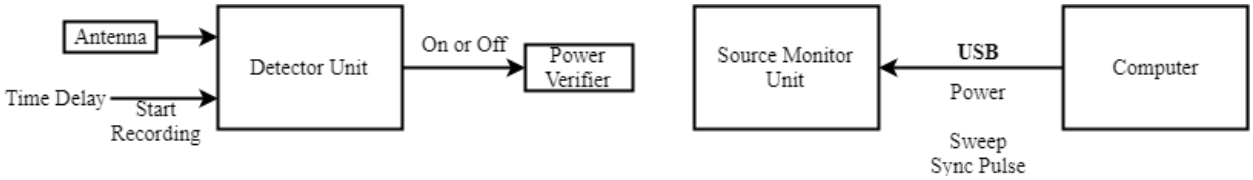


Figure 55: During Recording Setup

B 4.5.A Post-Recording Setup

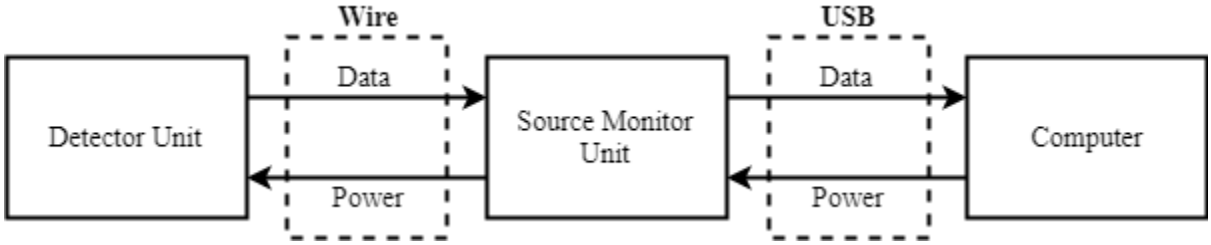


Figure 56: Post-Recording Setup

B 5. Background Knowledge/Phenomenology

Power Supply Selection, Detector Unit:

From ECE 285: Power (Watts)= Voltage (Volts) * Current (Amperes) [1]

Active components:

- NLB-300 RF Amplifier: Vd = 3.8 V, Icc = 50 mA (x2)
- ADL5906 RF Detector: Vd = 5 V, I = 70 mA (x1)

Total power consumption: 2*(3.8 V * 50 mA) + 1*(5 V * 70mA) = 730 mW

Add 20% margin for power: 730 mW * 1.2 = 876 mW.

For 5V Portable Battery Packs, storage is typically measured in milliampere hours (mAh).

W = V*A, thus W/V = A

There are 5V devices, so V = 5.

Thus, 1 mAh = 1 mWh/5

The requirements state the required run time is 8 hours.

To equate our data with the market: 876 mW = 876 mW * 8 hours / 5V

- Thus, we need a 1401.6 mAh battery.

Microstrip Impedance (RF PCB Characteristics):

Z_0 for RF PCB Design must equal 50 Ohms.

Z_0 is given by the formula: $Z_0 = \frac{87}{\sqrt{\epsilon_r+1.41}} \ln\left(\frac{5.98*h}{(0.8*w+t)}\right)$ [2]

w = trace width, t = trace thickness, h = dielectric thickness, ϵ_r = relative dielectric constant.

In mills, we could work with a minimum of 10 mills per GMU PCB Lab guidelines:

- w >= 10 mils

For the dielectric, we chose the RO4350B board material, as it met our frequency requirements.

- This yielded ϵ_r = 3.66

The copper cladding was 1 oz, which gave us our trace thickness:

- t = 1.4 mils

The board selected was 6.6 mils thick:

- h = 6.6 mils

Setting Z_0 to 50 and solving for w:

- w = 11.7754 mils

DC Blocking Capacitor

The capacitor is constructed from two electrically conducting metallic plates facing each other and separated by a dielectric. Applying DC voltage on the capacitor no conduction current flows through the capacitor if its shielding medium is perfect insulator. This is because there are no free charge carriers in such medium. Practically the real insulator contains very few charge carriers and therefore a very small leakage current passes in the capacitor depending on the conductivity of the insulator. If a time varying voltage is applied on the capacitor, a displacement current passes through the capacitor irrespective of the shielding medium. This current is called capacitive current [3]. This current flows because of changing electric displacement with time. The density of displacement current is equal to the rate of change of the displacement with time. The electric displacement is defined by D= ϵ*E, where ϵ is the dielectric constant and E is the electric field intensity. If the applied voltage varies with time, the E will be also time varying and displacement capacitive current will be present [3].

Current flow through the capacitor:

- $I = C\frac{dv}{dt}$
- Current = Capacitance * the rate of change in voltage.
- For DC voltage: $\frac{dV}{dt} = 0$. So a capacitor allows no current to flow through it for DC voltage.

The impedance of capacitor:

- $Z_{capacitor} = \frac{1}{j\omega C}$.
- For Low-Frequency RF and very low (nanometer scale) capacitance, impedance of the capacitor is very large. So, Capacitor shall block all frequencies near baseband.

Amplifier:

In order to increase the minimum detectable frequency, amplifier is needed. Basic operational amplifier has configuration shown in Figure 19:

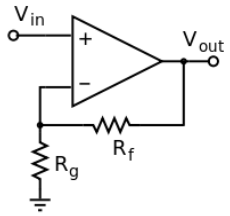


Figure 57: Basic Non-Inverting Feedback Amplifier Configuration [3]

- With the input signal, the output signal is amplified by the ratio of the R_f and R_g [3].

  Gain = $\frac{Vout}{Vin} = 1 + \frac{R_f}{R_g}$.

  $\text{Gain}_{\text{dB}} = 20log_{10}(Gain)$

For our purposes, Monolithic Microwave Integrated Circuit (MMIC) amplifier is needed to operate at microwave frequencies, from 100 MHz to 6 GHz, and device provides a characteristic impedance of 50 Ω. Cascading of MMICs does not require an external matching network which makes it easy to implement if multiple stages are needed.

- Looking at 13 dB gain will result in:

  $13\ dB = 20log_{10}(Gain) \rightarrow Gain = 4.467$

  $4.467 = 1 + \frac{R_f}{R_g}$ → Ratio of R_f and R_g = 3.467

Bias Tee:

This is a three-port device used with configuration shown in Figure 20:

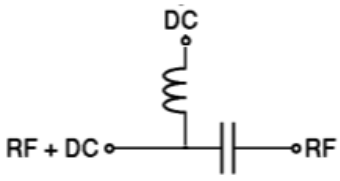


Figure 58: Bias Tee Configuration

Bias tee is used to control the flow of RF and DC signals in certain directions. The port denoted as DC will be connected to power supply, providing DC signal, that will be powering up the amplifier connected to RF+DC port. The RF signal will be flowing from RF+DC port to RF

port. The inductor will function as DC signal passer and RF blocker [1]. The capacitor will function as RF passer and DC blocker [1].

The inductor provides impedance that is variable to frequency:

$$X_L = 2\pi fL, \quad where\ f\ is\ frequency\ and\ L\ is\ inductance\ value$$

- With a given inductance value, higher the frequency, the higher the impedance is, and lower the frequency, the lower the impedance is. Frequency and impendence are directly proportional.
- The frequency range of operation shall be between 100 MHz to 6 GHz for RF, and the characteristic impedance, Z_0, shall be 50 Ω. To provide enough impedance to block RF, X_L must be much greater than Z_0, which means $X_L = 2\pi fL \gg Z_0$
- With Z_0 at 50 Ω and f = 100 MHz:

$$2\pi(100\ M)L \gg 50 \rightarrow L \gg 79.6\ nH$$

- For DC signal operating at 0 Hz:

$X_c = 2\pi(0)L = 0$, therefore, inductor provides no impedance for DC signal.

The capacitor provides impedance that is also variable to frequency:

$$X_C = \frac{1}{2\pi fC}, \quad where\ f\ is\ frequency\ and\ C\ is\ capacitance\ value$$

- Frequency and impedance are inversely proportional.
- To provide minimal impedance for RF to pass, X_C must be much less than Z_0, which means $X_C = \frac{1}{2\pi fC} \ll Z_0$
- With Z_0 at 50 Ω and f = 100 MHz:

$$X_C = \frac{1}{2\pi(100\ M)C} \ll 50 \rightarrow C \gg 31.8\ pF$$

- For DC signal operating at 0 Hz:

$X_C = \frac{1}{2\pi(0)C} = \infty$, therefore, capacitor is a DC signal blocker.

Bias Current Resistor:

Due to the nature of the component chosen for amplifier, current needs to be controlled for the correct supply of voltage and current to operate the amplifier. Biasing can be done with a resistor [3].

- $V = IR$

- With constant voltage, increasing the resistance value will reduce the current, and decreasing the resistance value will increase the current.
- Typical bias configuration is displayed by Figure 21:

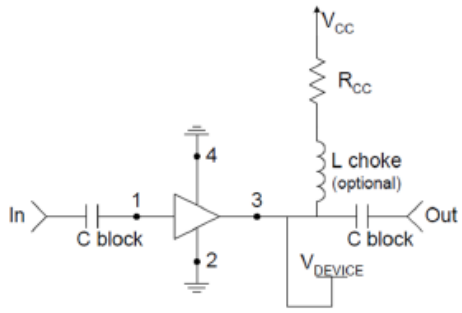


Figure 59: Bias Configuration with Amplifier and Bias Tee [4]

- Based on the specification of the amplifier, voltage of the device (V_{DEVICE}) is 3.8 V, and operating current (I_{CC}) is 50 mA. The resistor value needed can be calculated by:

  $R = \frac{V_{CC} - V_{DEVICE}}{I_{CC}}$, where V_{CC} of 5 V shall be supplied.

  $R = \frac{5 - 3.8}{0.05} = 24\ \Omega$

Analog to Digital Quantization:

The process of quantization converts a continuous signal into discrete set of values and determines the resolution of the digital data representation of the analog signal. With analog signal, number of amplitude levels to be represented with the sampled times is determined [5]. Example is shown in Figure 22 with arbitrary signal and levels.

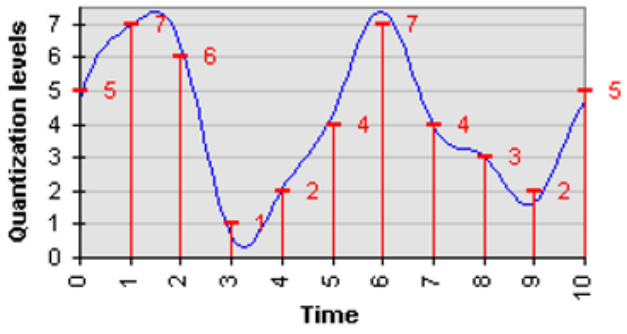


Figure 60: Quantization Levels

This example provides 8 different levels to represent the discrete time data. Each sampled time will look at the levels and determine which level is closest to represent the amplitude. For example, at time 9, the analog signal is between level 1 and 2 but closer to level 2, and there for will be represented by 2. The more levels are present, the more accurate the amplitude of the actual analog signal can be represented. The levels correspond to how many bits are needed [5].

- $\#\ of\ bits\ needed = log_2(\#\ of\ levels)$

  For this case, 3 bits are needed, and the representation is shown in Figure 23:

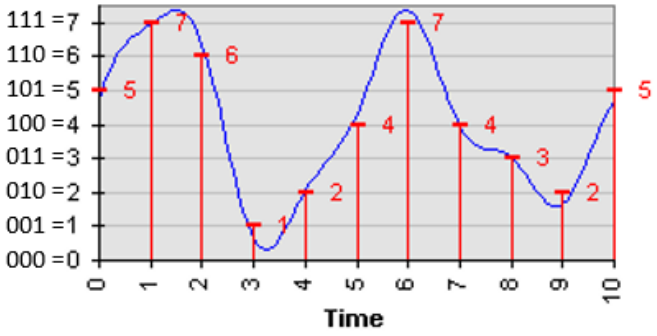


Figure 61: Quantization with 8 Levels

- For our case, 12-bit ADC provides:

  $12 = log_2(\#\ of\ levels)$ → $\#\ of\ levels = 4096$, which shall give sufficient resolution.

Decibel and Decibel-milliwatt Scale

The term decibel (dB) is used for defining gain of a system. As it is with our system, amplifier gain is a ratio of the output and the input power of signal defined in terms of dB as [3]:

- $dB\ scale = 10log_{10}\left(\frac{P_{output}}{P_{input}}\right)$

  The ratio of the output and the input defines the gain of the system.

Decibel-milliwatts (dBm) is the level of signal strength used to define a power ratio expressed in dB with reference to one milliwatt where strength doubles every 3 dB [5]:

- $dBm\ scale = 10log_{10}\left(\frac{P}{1\ mW}\right)$, or simply $10log_{10}(signal\ strength\ in\ mW)$
- Since the device shall have minimum detectable power of -30dBm:

  $$-30\ dBm = 10log_{10}(signal\ strength\ in\ mW)$$
  $$Signal\ strength\ in\ mW = 10^{-3} = 0.001\ mW\ or\ 1\ \mu W$$

  1 μW is the minimum detectable power

- $0\ dBm = 10log_{10}(signal\ strength\ in\ mW)$

  $$Signal\ strength\ in\ mW = 10^{0} = 1\ mW$$

  1 mW corresponds to 0 dBm

B 6. Detailed Design

B 6.1 Overall Design

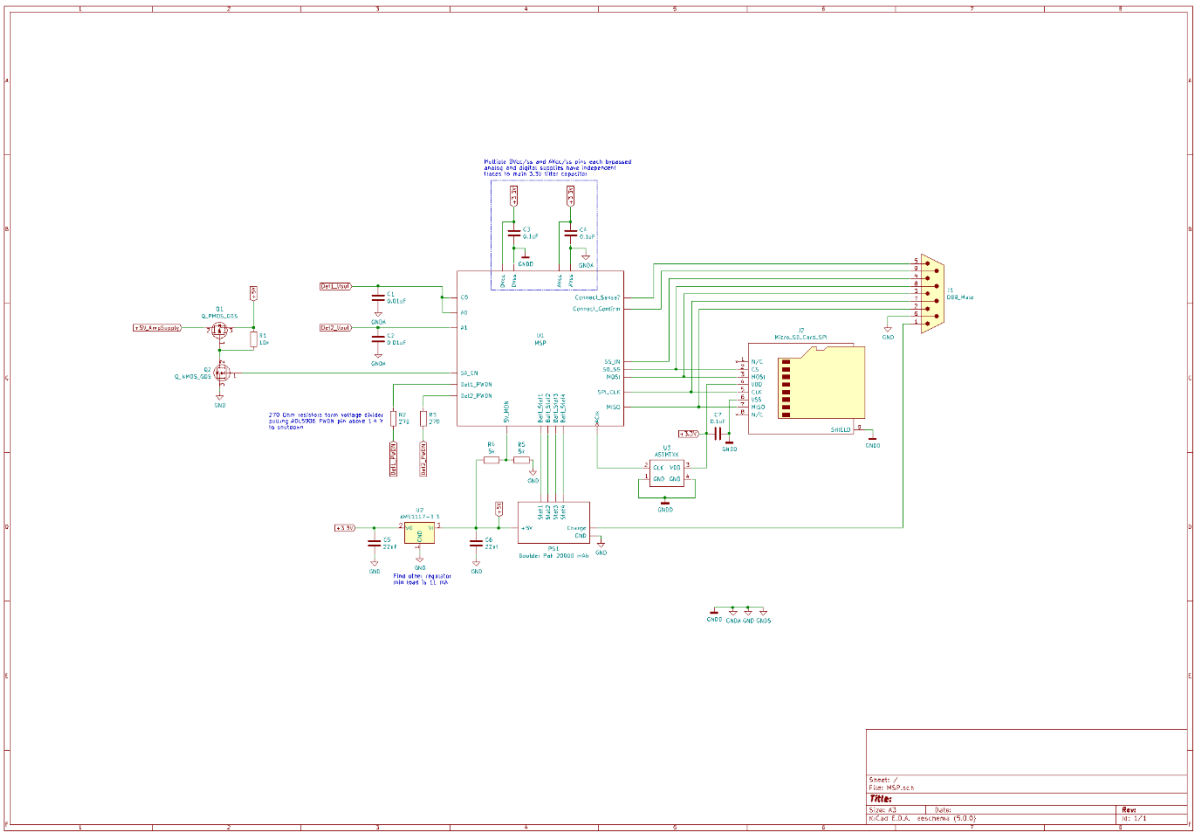


Figure 62: Detector Unit MSP Schematic

The various power supply pins of the MSP microcontroller are bypassed to their appropriate analog or digital grounds. The analog inputs from the two RF detectors are locally bypassed by 0.01µF capacitors to reduce noise. The 5 volt supply to the RF amplifiers is sourced through a P-channel MOSFET to minimize the on-state voltage drop. This transistor's bias is controlled by a pull-up resistor and an N-channel MOSFET to allow the 3.3 volt signal from the MSP to control the 5 volt line. The two detectors are powered down by pulling the TADJ/PWDN pin above 1.4 volts. The 270 Ohm resistors reduce the current consumption of the shutdown signals and provide some noise isolation for the TADJ voltage [6].

When the detectors are to be powered on, the shutdown pins on the MSP are placed in a high-impedance state. A voltage divided reduces the 5 volt supply to 2.5 volts which is fed to the analog comparator in the MSP to detect low voltage conditions. The 32 kHz clock signal is

generated by a temperature compensated high precision oscillator. An external clock source was chosen, as opposed to using the crystal resonator driving circuit integrated into the MSP, because the accuracy of the clock source for the real-time clock is critical for accurately determining the frequency that was transmitted during each measurement.

Designing a crystal oscillator circuit with proper capacitive loading and software-controlled temperature compensation was considered to high risk given the project timeline and availability of an inexpensive alternative. The measurement data gathered by the detector MSP is written to a micro-SD card via SPI and is read by the source monitor via SPI. The interface connector to join the source monitor and the detector is a standard DB-9 connector. An RF shield is available to prevent the RF environment from coupling into the detector circuitry when the devices are disconnected during a test. Connections are available for the SPI interface including slave select for the SD card and the detector MSP. Additional connections are used for power the charge the battery and to determine if the devices are connected.

The connection sense pin is configured as a digital input with an internal pull-down resistor. When the devices are connected, this line is pulled high signaling the detector MSP to reconfigure as an SPI slave to prevent to masters from driving the SPI bus. Once this is complete, the detector drives the connect confirm line, signaling the source monitor MSP it is safe to drive the bus. The battery to power the detector is a USB based portable power pack with pass through charging capability. It has charge management circuitry built in and includes a 5-volt power supply. The status signals originally used to drive LEDs on the power pack are connected to digital inputs on the detector MSP, so that it can monitor the charge status. A 3.3-volt low drop-out regulator is used to provide the power needed for the MSP, SD card, and the high precision oscillator. While its voltage regulation accuracy is important, it is not critical to analog voltage measurement accuracy, which uses the internal voltage reference source in the MSP.

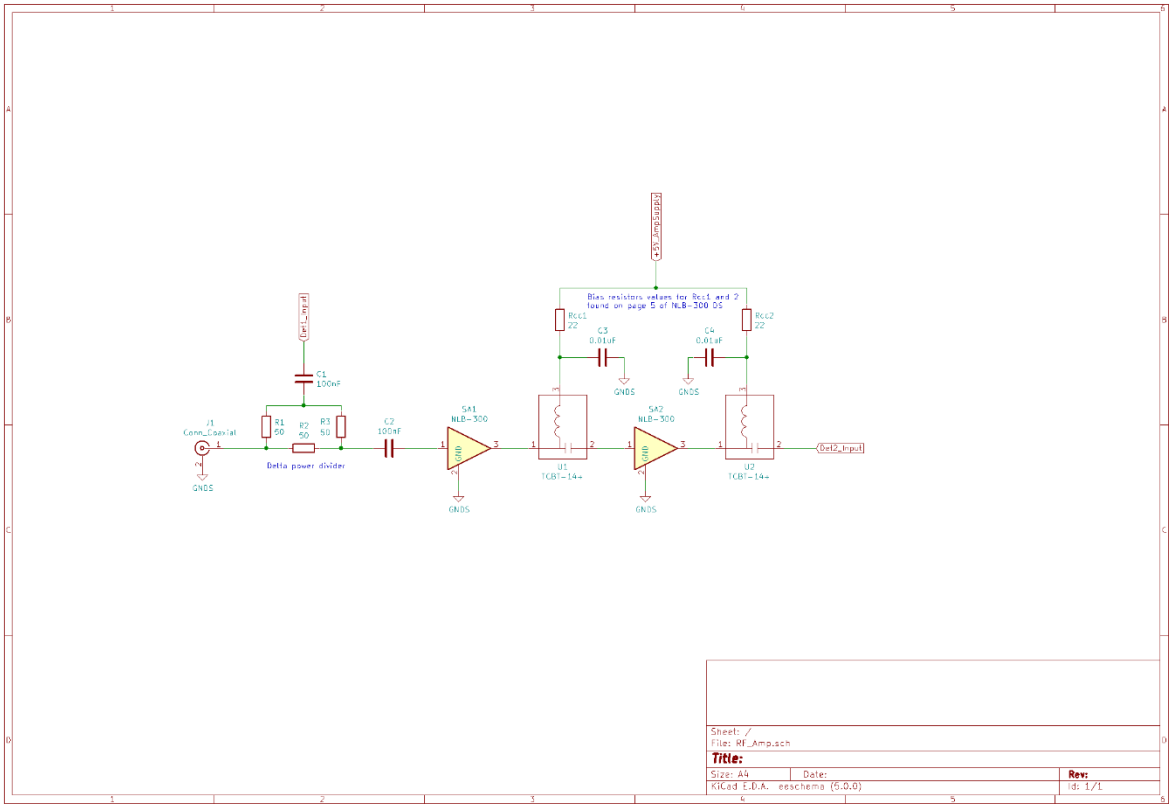


Figure 63: RF Amplifying Stage Schematic

A standard SMA coaxial connector is used for the RF input signal. This signal is split equally between the low gain detector input and the low noise amplifier input using a 6 dB resistive divider. A resistive divider is used despite its inherent power inefficiency because of its broadband frequency response. A reactive 3 dB power divider with even division and high return loss would be far more difficult to design. A delta resistive divider was chosen over a star divider due to the greater availability of 50 Ohm resistors compared to 16.3 Ohm resistors. Each NLB-300 provides fixed gain and are cascaded so that the total gain is a large portion of the dynamic range of the detectors, maximizing the increase to the system dynamic range provided by the two gain stages. DC power is provided to the amplifiers by biasing the output lines. Bias tees are used to isolate the DC power from the RF signal. The 22 Ohm common collector resistors are used to set the operating point of the amplifiers [4].

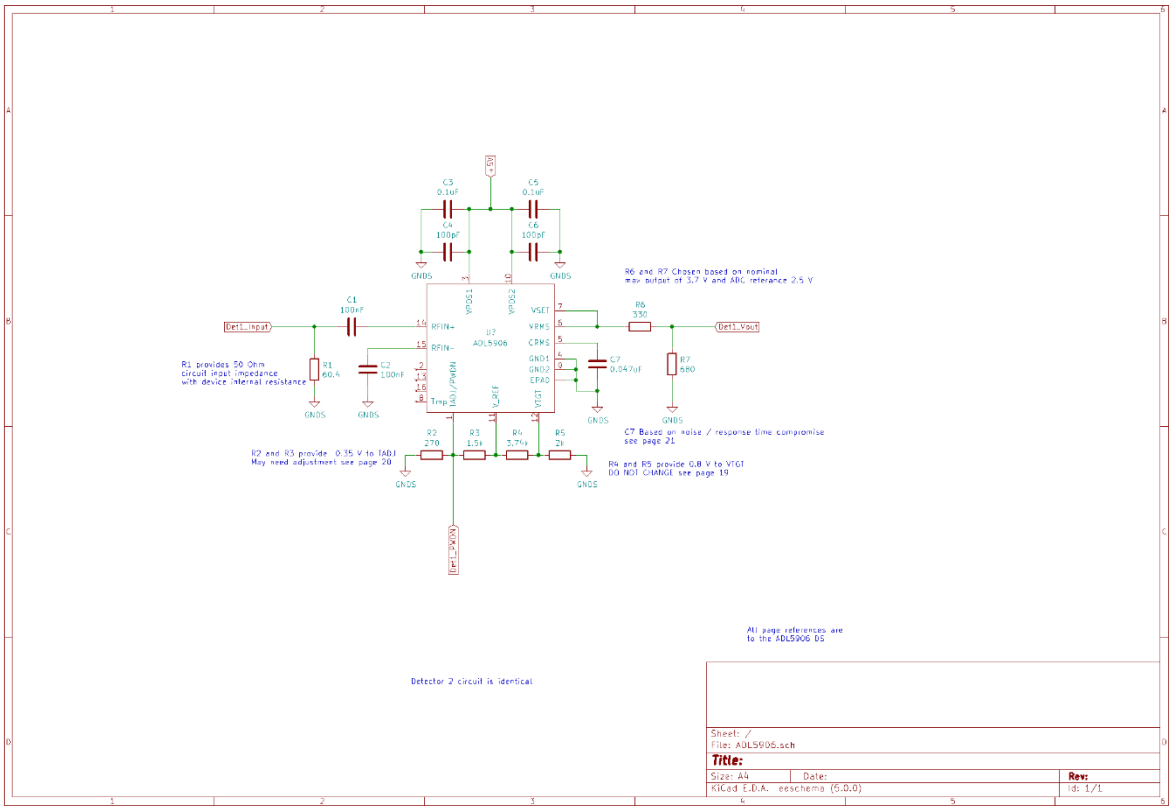


Figure 64: Detector Chip ADL5906 Schematic

The ADL5906 produces an analog output voltage that is linearly proportional to the RF power received in dBm. The 60.4 Ohm input shunt resistor provides a 50 Ohm input match when combined with the internal input resistance of the ADL5906. Capacitor C1 provides DC blocking for the bias on the input line generated by the ADL5906. Capacitor C2 provides a ground path for the RF signal from the negative differential input, allowing single ended operation for the unbalanced input. Resistors R2 and R3 divide the reference voltage, providing the temperature adjust set voltage. Resistors R4 and R5 divide the reference voltage, providing the squaring amplifier gain setting. Capacitor C7 provides output voltage averaging, the value chosen provides a compromise between noise immunity and response time. Resistors R6 and R7 divide the output voltage producing a voltage from 0 to 2.5 volts from the 0 to 3.7 volt output signal. This is to keep the analog voltage within the range of the ADC in the MSP [6].

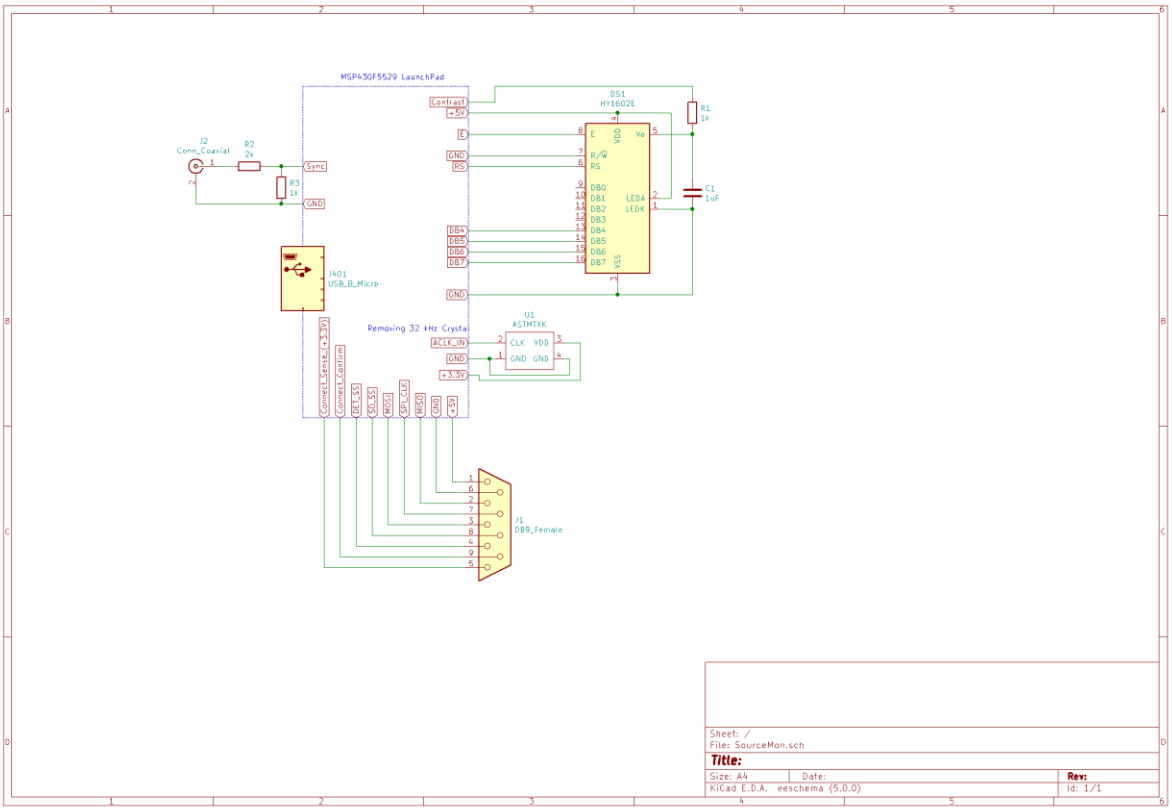


Figure 65: Source Monitor Unit MSP Schematic

The MSP430F5529 LaunchPad is used as the control board in the source monitor. The LaunchPad already has a 3.3 volt regulator and proper bypassing for the MSP. It has the micro USB connector needed to interface with the test computer. It already has pin headers to connect to the 1602 LCD and the interface connector. It already has the high speed oscillator needed for USB communication. The only modification necessary is the replacement of the 32 kHz crystal with the high precision 32 kHz oscillator.

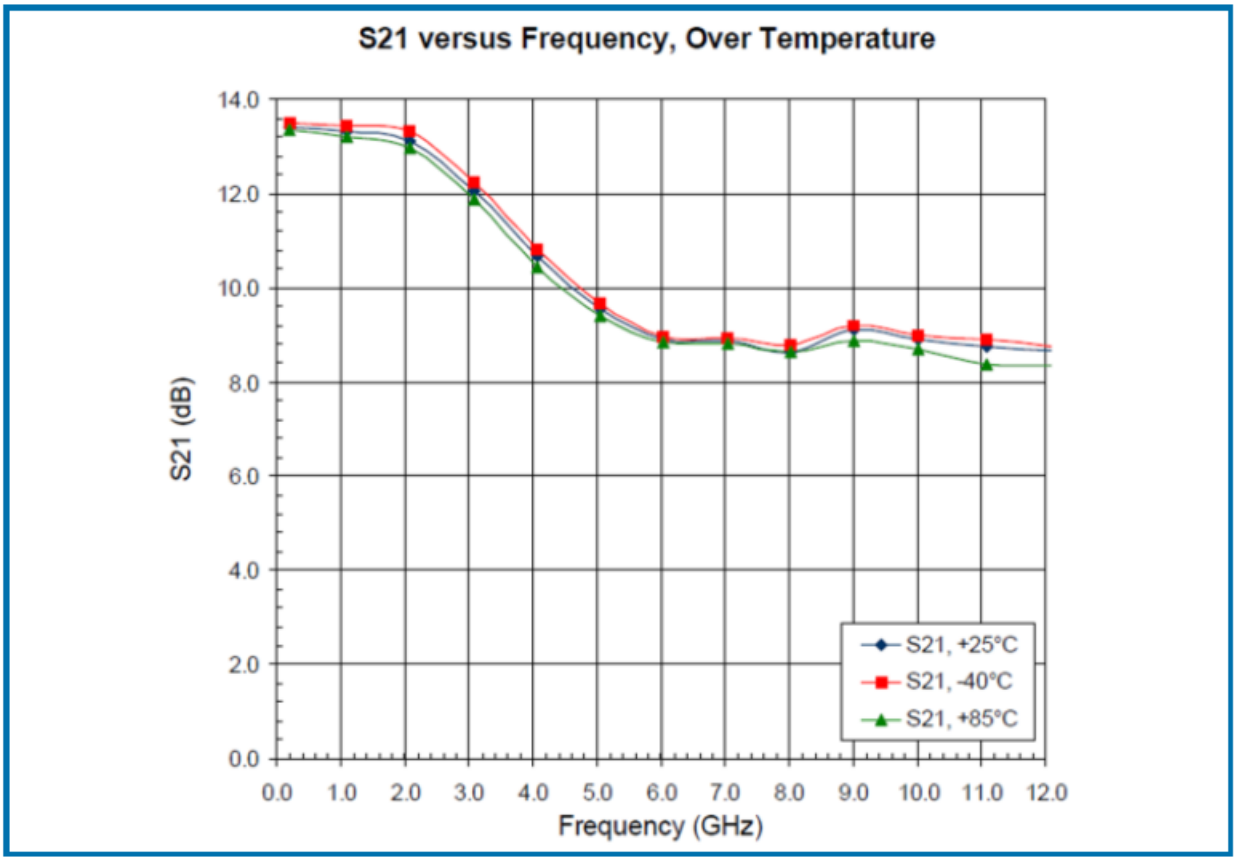


Figure 66: NLB-300 Gain vs Frequency [4]

100 MHz			
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C	62	dB
Maximum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm	2	dBm
Minimum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm	−60	dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 0.35 V		
	−40°C < T_A < +85°C; P_{IN} = 0 dBm	−0.8/+0.2	dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm	−0.8/+0.4	dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm	−1.3/+0.2	dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm	−1.2/+0.6	dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm	59	mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm	−64	dBm
5800 MHz			
±1.0 dB Dynamic Range	CW input, T_A = 25°C	57	dB
Maximum Input Level, ±1.0 dB	Calibration at −50 dBm, −40 dBm, and 0 dBm	3	dBm
Minimum Input Level, ±1.0 dB	Calibration at −50 dBm, −40 dBm, and 0 dBm	−54	dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 1 V		
	−40°C < T_A < +85°C; P_{IN} = 0 dBm	−2.4/+0	dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm	−1.4/-0.2	dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm	−3.6/+0	dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm	−2.1/-0.2	dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm	42	mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm	−60	dBm

Figure 67: ADL5906 High and Low Frequency Response [6]

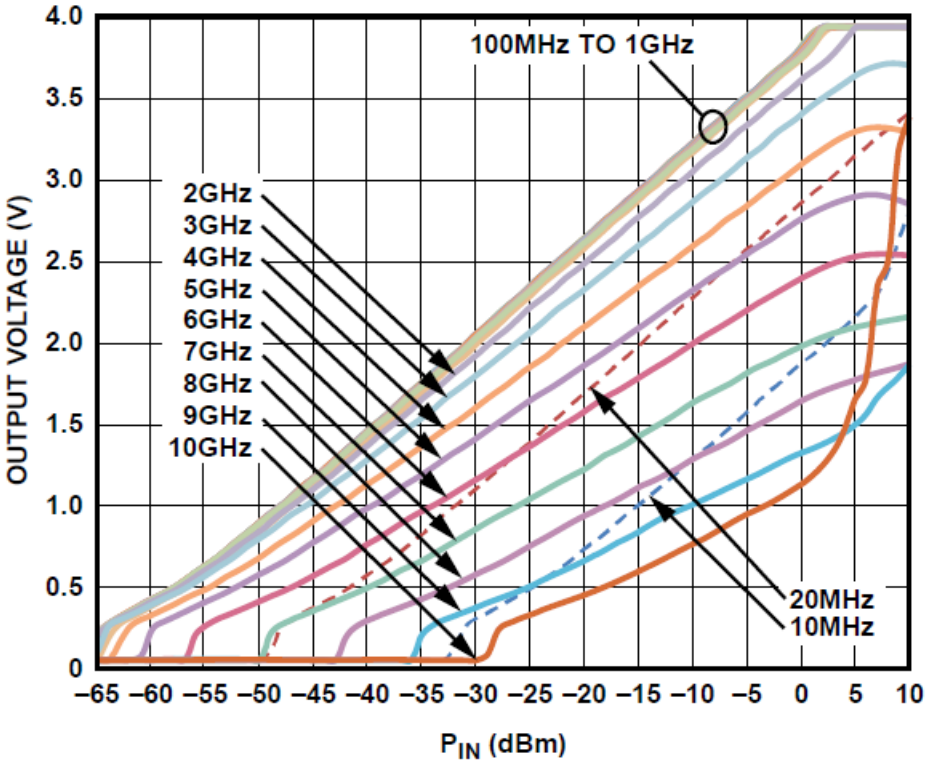


Figure 68: ADL5906 Frequency Response [6]

Frequency (MHz)	Low Gain Input Range (dBm)	High Gain Input Range (dBm)	Total Range (dBm)	Dynamic Range (dB)
100	-54 to +8	-80 to -18	-80 to +8	88
5800	-48 to +9	-66 to -9	-66 to +9	75

The detector output voltage slope is 42 millivolts per dB at 5800 MHz. Using a 12-bit ADC with a 2.5 volt reference, the voltage resolution is 611 micro-volts. This corresponds to a power resolution of better than 0.02 dB.

B 6.2 Detailed Description of Components

RF power detector: ADL5906

The ADL5906 was chosen for the RF power detector chip. Its frequency range of operation is specified as 10 MHz to 10 GHz, which covers the range of operation of the project. While its performance near 10 GHz is diminished, its performance up to 6 GHz is well within the requirements needed. The detectable power range at 6 GHz is -54 dBm to +3 dBm, which even with input loses, provides sufficient sensitivity and dynamic for this application. Using square law detectors, it provides a linear output voltage with respect to power received in dB. This simplifies the analog to digital conversion when compared to diode detectors that provide exponential output voltages. The exponential detectors require a linearizing circuit, or variable gain dc amplifiers to provide equal resolution over the range of operation. The ADL5906 requires a single 5 volt supply, and has a power down mode, so power supply requirements are simple. Broadband input impedance matching is achieved using a single external resistor, mitigating the need to design a complex impedance matching network, as is necessary for similar devices.

MMIC Amplifier: NLB-300

To provide input signal gain, A Monolithic Microwave Integrated Circuit (MMIC) amplifier was chosen. The MMIC amp is internally matched to 50 Ohms at the input and output. This mitigates the need to design broadband matching networks to compensate for the complex S_{11} and S_{22} impedances of discrete RF amplifier transistors. The specific device chosen is the NLB-300. It is a four-terminal device with two grounds, input, and output. It is powered through a bias tee in the output line, requiring five volts. This makes it power supply compatible with the ADL5906. It is a fixed gain device providing between 8.9 and 13.0 dB of gain in the relevant frequency range. It has a low noise figure of 4.9 dB and a high third order intercept of greater than 27 dBm.

Source Monitor Microcontroller: MSP430F5529

The MSP430F5529 microcontroller was selected for use in the source monitor. It has an SPI peripheral needed to communicate with the detector controller and access the recorded data from SD cards. It has a USB communications peripheral needed to communicate with the test control computer. It has a real-time clock needed to provide the time events occurred. An interrupt generating digital input will be used to detect the sync pulse from the RF source. A PWM capable

timer peripheral will be used to generate the contrast signal to the LCD display. Eleven digital I/O pins interface with the 1602A LCD display.

Source Monitor Display: 1602A LCD

The 1602A LCD display was chosen for the display on the source monitor because it is widely available and libraries to control it are already written.

Detector Device Microcontroller: MSP430FR6989

The MSP430FR6989 was chosen for the microcontroller in the RF detector device. It has a multi-channel twelve bit analog to digital converter needed to measure the voltage output of the detector ICs and the level of the 5-volt supply line. It has a RTC to provide the time stamp data for each sample. It has an SPI peripheral needed to communicate with the source monitor and the SD card used to store measurement data. It has sufficient digital I/O pins to control the power-down of both detectors and the input signal amplifier and to interface with the 5-volt power supply for charge status. While the MSP430FR6989 may have more capabilities than are used in this application, the team already has experience programing them, the team already has development boards in their possession, the additional cost compared to a less capable device is trivial for a non-production project like this one, and an unfamiliar device puts the project schedule at risk.

Low Frequency Clock: ASTMTXK-32.768kHz-N-G MEMS Oscillator

The ASTMTXK-32.768kHz-N-G MEMS Oscillator was chosen as the low frequency clock source for both the RF detector and the source monitor. It is a low power clock source used to provide the input clock to the RTC peripherals needed for data time-stamping. It is powered by 3.3 volts with a quintessential current of 1.52 micro Amps. It is internally temperature compensated providing a temperature stability of ± 5 ppm. The accuracy and stability of this clock source is greater than what we believe we can achieve using a discrete crystal and the drivers built into the MSP430 microcontrollers.

B 6.3 Description of Software

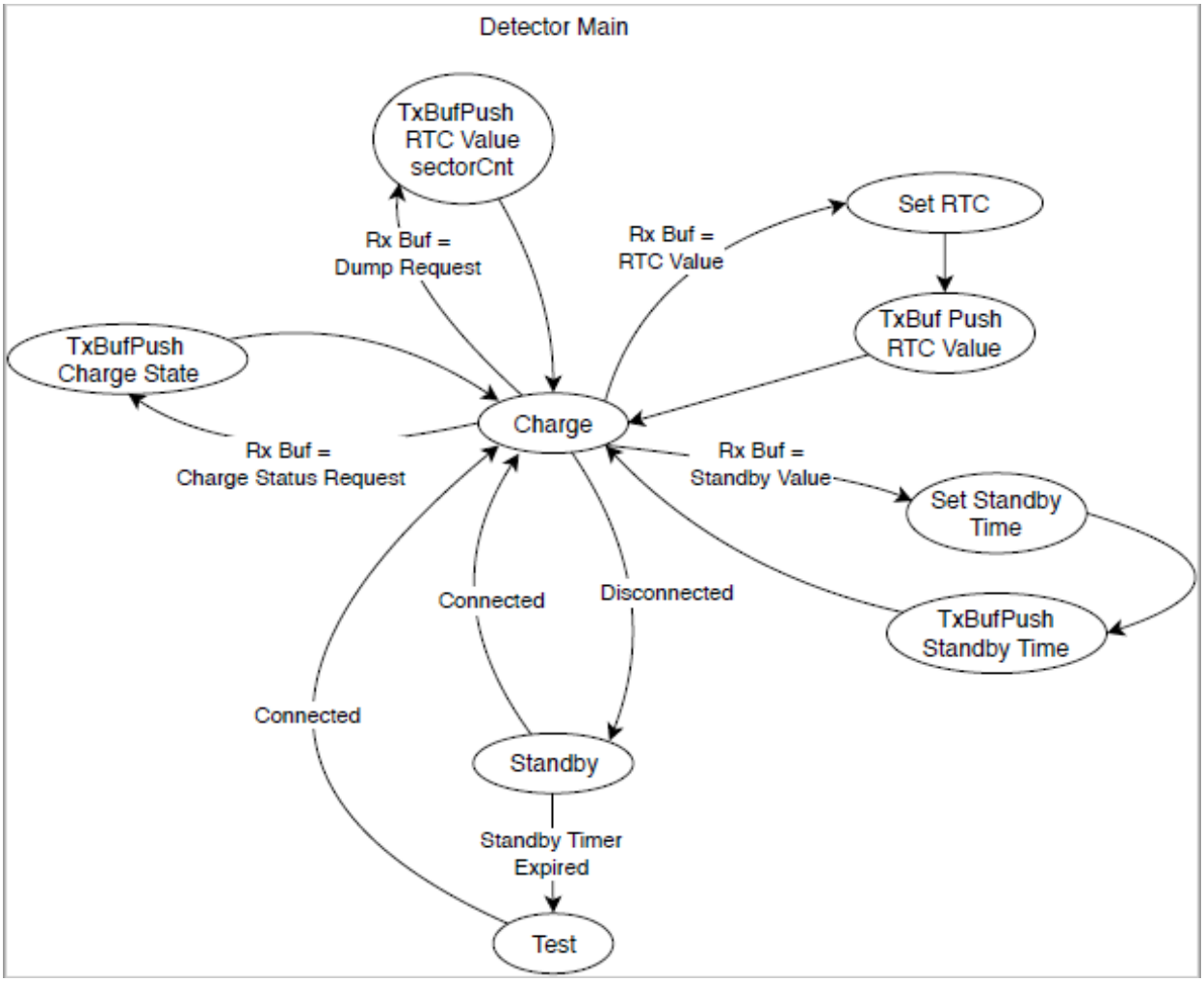


Figure 69: Main State Diagram of Detector Unit

When the detector is connected to the source monitor it is in the charge state. The source monitor will regularly poll the detector via SPI for the current charge state. When the source monitor sends the test configuration parameters, being the current time and the standby delay time, the detector echoes the values to ensure they were properly received. When the detector is disconnected from the source monitor, the connection sense pin changes state, triggering an interrupt. The interrupt service routine starts the standby timer. Once the standby timer expires, the detector changes to the test state. The ADC and RF amplifier are enabled as well as a sample timer interrupt. The detector remains in this state until it is reconnected to the source monitor.

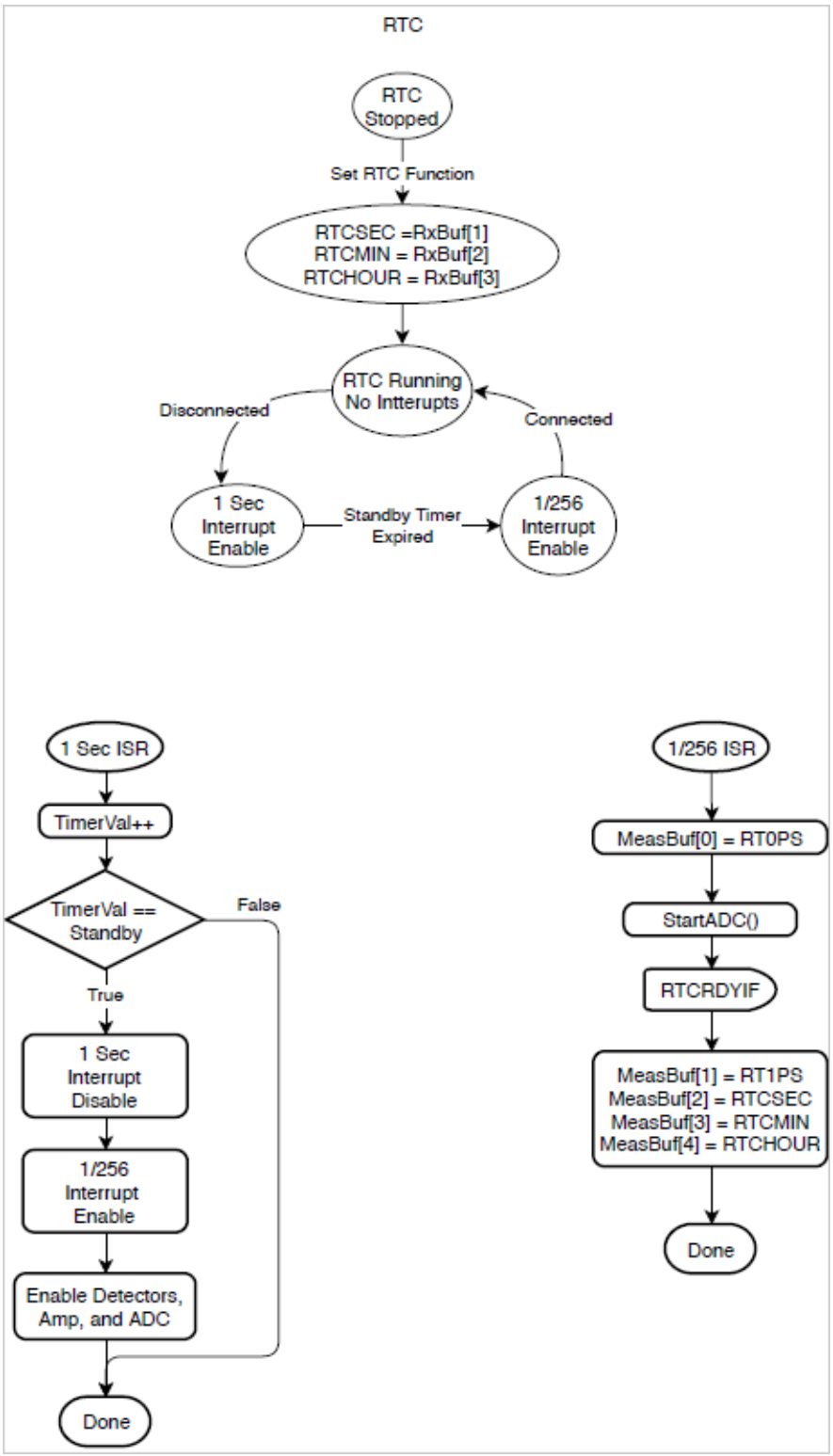


Figure 70: Detailed State Diagram and Flow Chart of RTC (Detector Unit)

Once the RTC is set, it runs continuously. When the detector is disconnected from the source monitor, the standby timer is started by enabling the one second interrupt from the RTC.

While it is inefficient to use a one second interrupt to determine the standby delay as opposed to the RTC alarm peripheral, it allows code reuse from the source monitor, which uses the one seconds interrupt to update the LCD display showing the remaining time. Once the standby timer reaches the standby delay time, the one second interrupt is disabled, the ADC, detectors, and amplifier are enabled, and the sample timer is enabled by enabling the two-hundred fifty-sixth of a second interrupt. The sample timing interval is derived from the RTC prescaler so it will be synchronized to the other RTC values. When the interrupt triggers, the least significant prescaler value is stored in the buffer, the ADC sample is started, by this time the any changes to the more significant RTC registers should have rippled through, so the RTC ready blocking loop should be inconsequential in the ISR. Then, the rest of the RTC values are stored in the measurement buffer

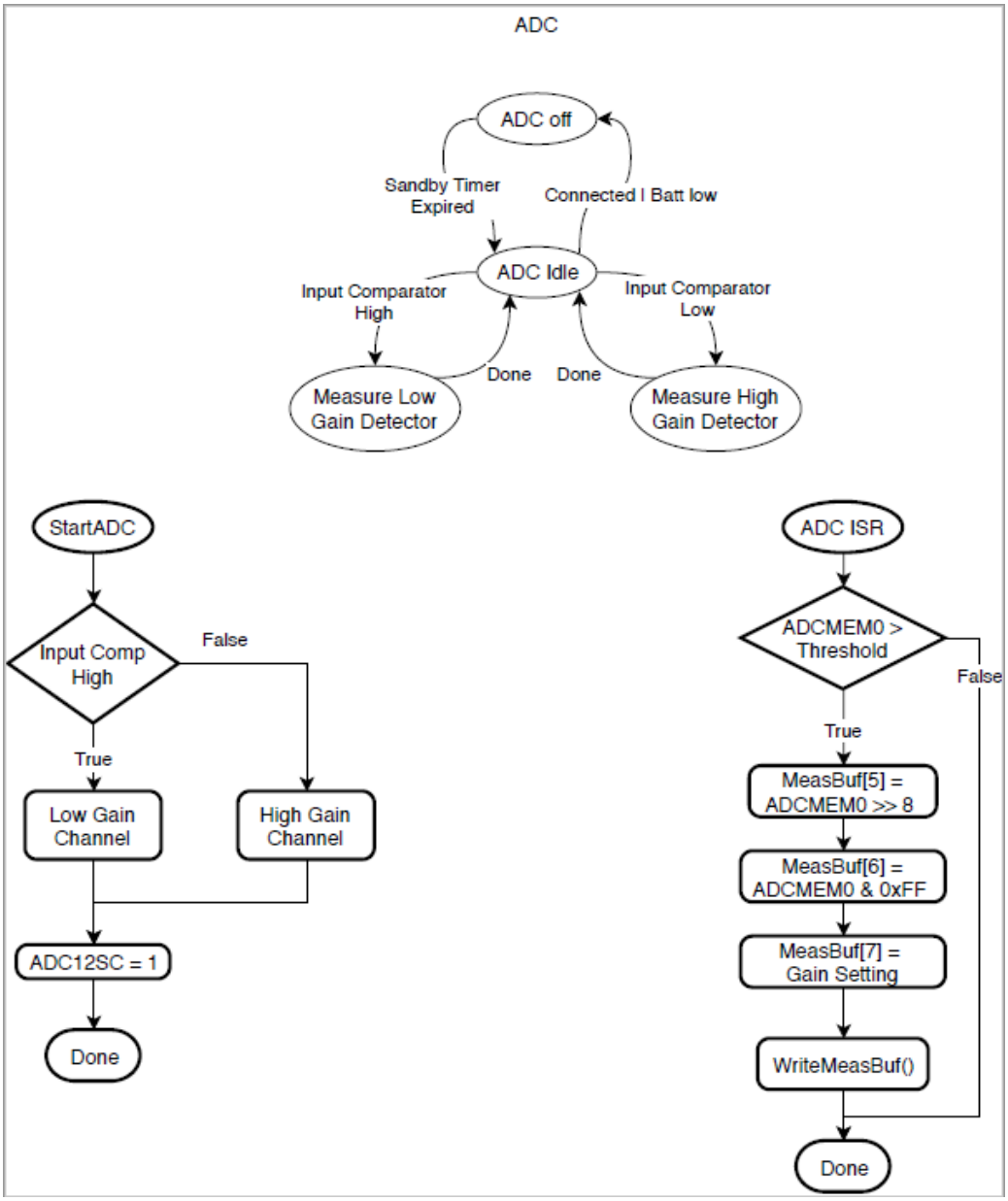


Figure 71: Detailed State Diagram and Flow Chart of ADC (Detector Unit)

The ADC is powered down until the detector is in the test state. When the sample timer ISR calls the StartADC function, the comparator connected to the low-gain detector is used to determine if the low or high-gain ADC channel should be converted. Then, the ADC is triggered via the software trigger bit. When the conversion is complete the ADC ISR is triggered. If the measured value is below the noise threshold, it is not recorded and the time-stamp values in the measurement buffer will be over written by the next sample. If it is above the noise threshold, the twelve-bit ADC value is put in the measurement buffer, along with the gain setting used. The function the writes the buffer values to memory is then called.

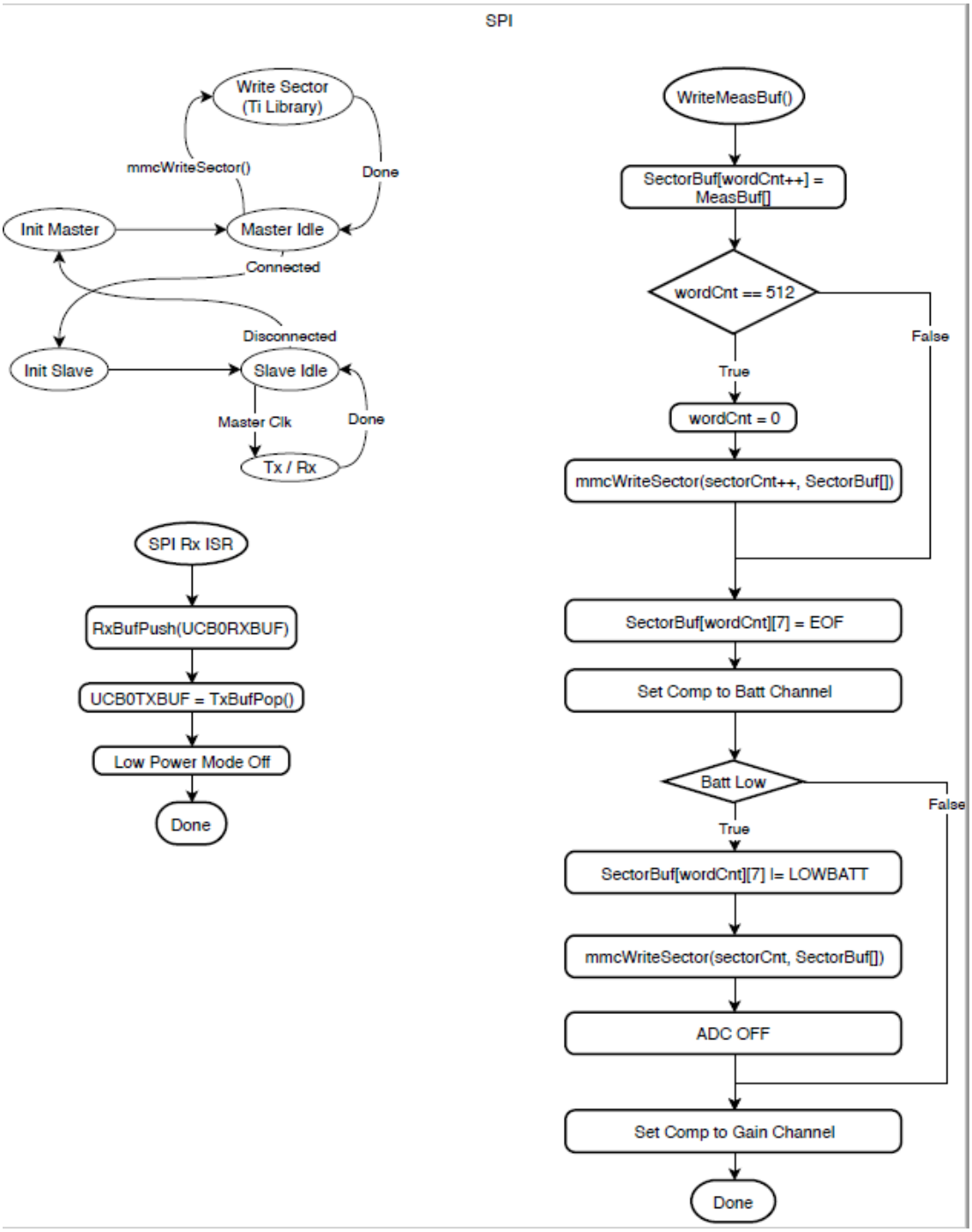


Figure 72: Detailed State Diagram and Flow Chart of SPI (Detector Unit)

When the detector is connected to the source monitor, it is configured as an SPI slave. Otherwise it is configured as a SPI master to write data to the SD card. When configured as a slave, data is moved in and out of two FIFO buffers, one for transmit and one for receive. When configured as a master, data is written to the SD card using a library available from Texas Instruments, referenced in application not SLAA281C. Data is written in five-hundred and

twelve-byte sectors. This is accomplished using the DMA peripheral, but is transparent to the end-user. The write measurement buffer function adds the last measurement buffer to the sector buffer. If the sector buffer is full, the sector is written to the SD card. This process may take longer than the time until the next measurement, but the data in the beginning of the buffer that will be overwritten will already be loaded into the SD card with a safe time margin. After each measurement is loaded into the sector buffer, the end of data marker is set in the following location indicating the last valid data. This marker is overwritten by the gain setting when a new measurement is taken. The comparator is briefly connected to the battery status input. If the battery voltage is below the threshold, in addition to the end of data marker, a low batter marker is placed in the data buffer and the last sector is written. The ADC is then disabled halting further measurements until the detector is recharged.

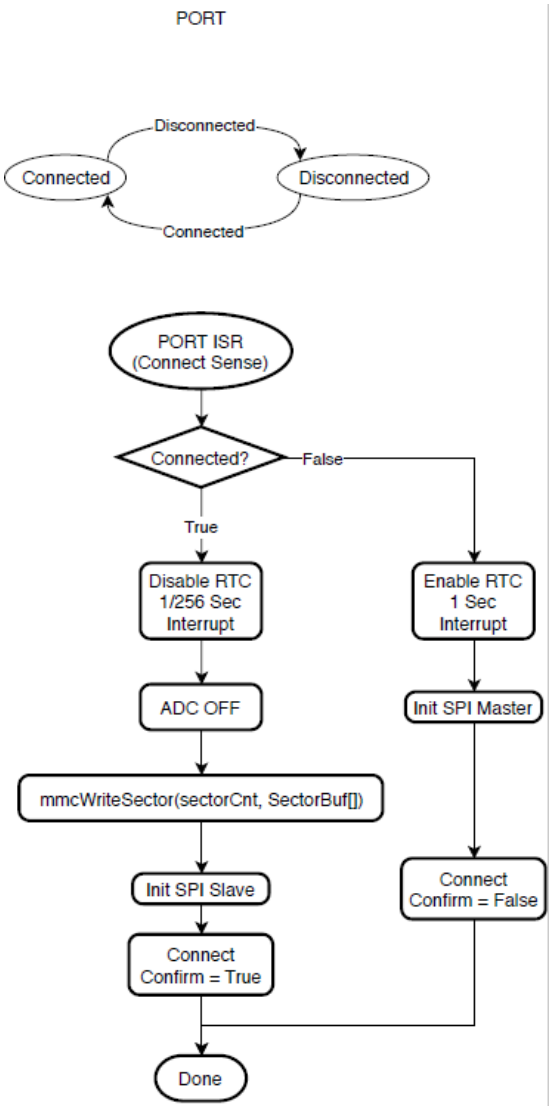


Figure 73: Detailed State Diagram and Flow Chart of Port (Detector Unit)

In order to detect when the devices are connected, a digital input with an internal pull-down resistor is routed to the interface connector. When it is plugged in, three volts from the source monitor pulls the line high and triggers an interrupt. The sample timer is stopped, the ADC is shutdown, the sector buffer is written to the SD card, and once complete, the SPI peripheral is configured in slave mode for communication with the source monitor. Once the SPI peripheral is reconfigured, a digital output routed to the interface connector signals that the detector is ready for the source monitor to become the master on the SPI bus. When an interrupt occurs because the devices are disconnected, the standby timer is started and the SPI peripheral is configured as the master to write data to the SD card. The connection confirmation line is set to false in preparation for the next connection.

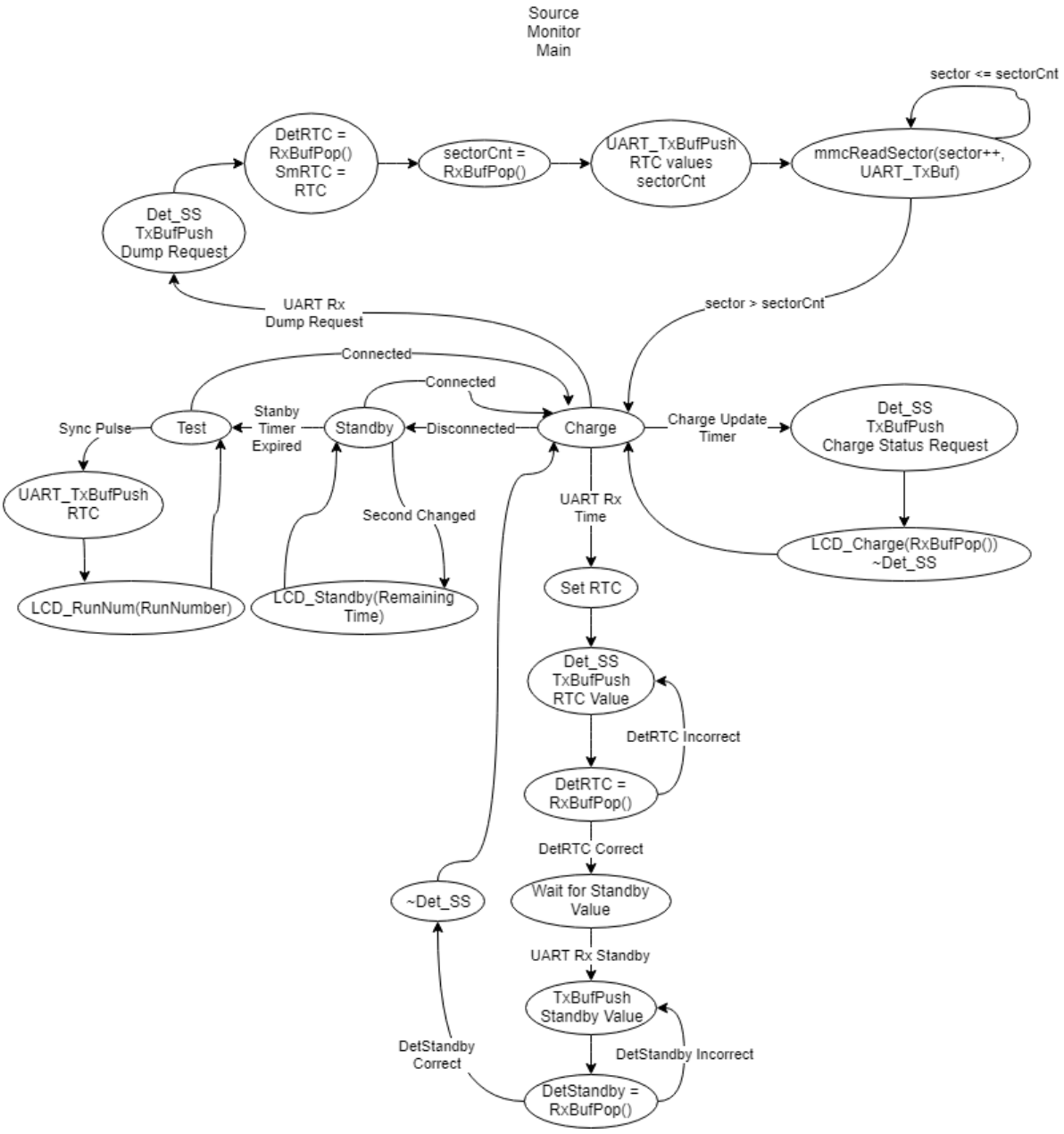


Figure 74: Main State Diagram of Source Monitor Unit

When the detector and source monitor are connected, the source monitor is in the charge state. It polls the detector for the current charge status at regular intervals (every two seconds) and updates the LCD with the current state of charge. When a command arrives from the test computer via the emulated COM port, it is placed in the UART_Rx FIFO buffer and the source monitor is taken out of low power mode. If the command is to set the RTC, the time value provided by the test computer is loaded into the RTC registers and the SPI_Tx FIFO buffer to be set to the detector. The detector will echo the received time value to ensure proper reception, and

it will be retransmitted if necessary. Following the time value, the standby delay is sent form the test computer and is again passed to the detector, which echoes for verification. When the devices are disconnected, the standby timer is started. The amount of time remaining in standby is displayed on the LCD and updated each second. When the Standby timer expires, the source monitor changes to the test state. The time, from the RTC, of each rising edge on the sync pulse input pin is stored in a buffer in memory. The LCD displays the number of pulses received to compare the run number detected with the run number transmitted. When the devices are reconnected, the source monitor returns to the charge state. When the source monitor receives a data request from the test computer, retrieves the detector RTC value and stores a copy of its own for clock drift detection. It then retrieves the number of sectors written to the SD card from the detector. It transmits these values to the test computer and then uploads the data recorded on the SD card to the test computer. Once the detector data is uploaded, the source monitor uploads the time stamps of the sweep sync pulses.

The 1602A LCD is controlled using libraries provided by the University of Texas El Paso. The emulated COM port via USB in the MSP430F5529 is controlled using the Simple USB Back Channel libraries provided by Texas Instruments.

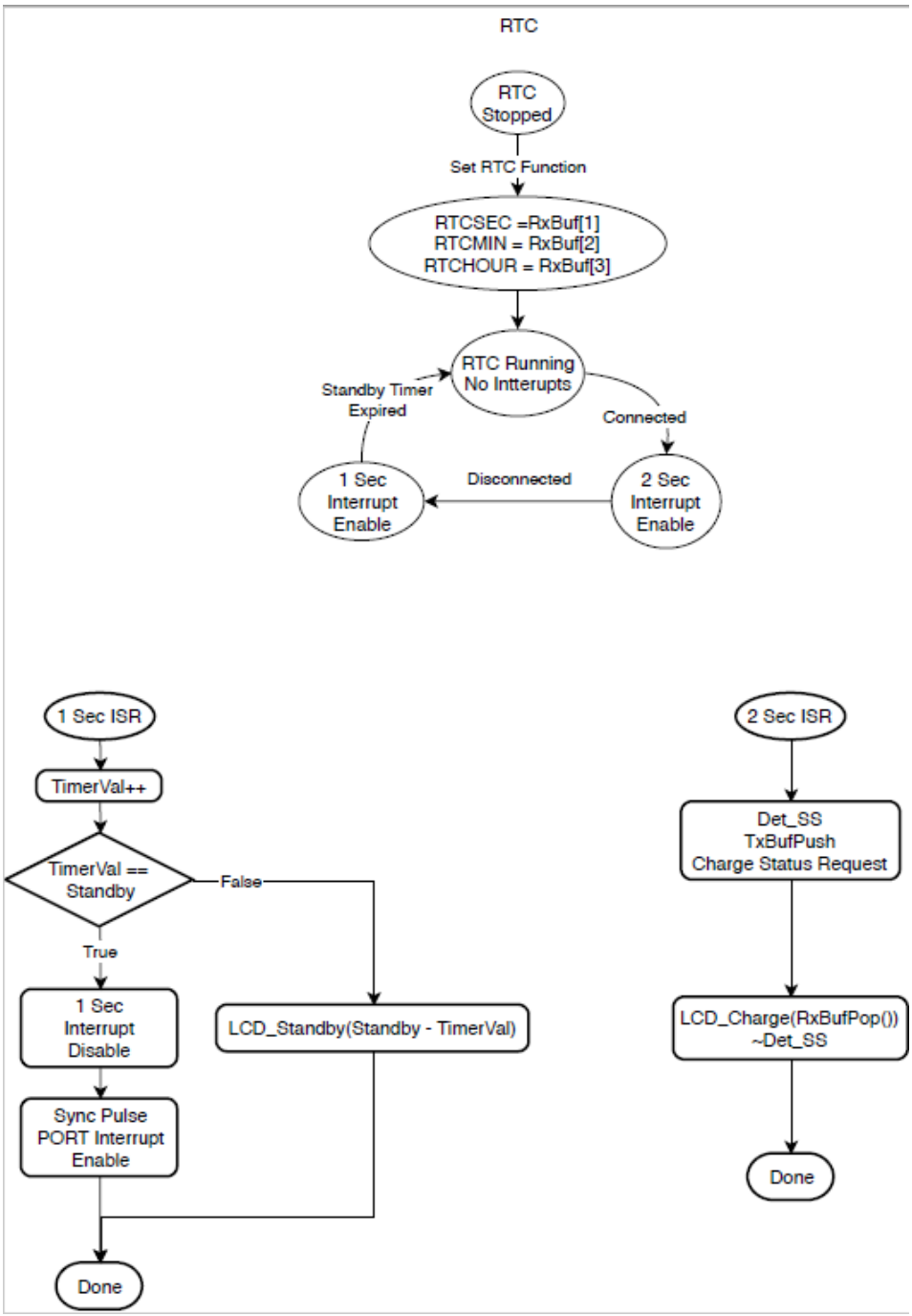


Figure 75: Detailed State Diagram and Flow Chart of RTC (Source Monitor Unit)

The RTC peripheral is used to generate the time stamps of each received sweep sync pulse. It is also used to measure the standby delay, and the charge status update interval. While the RTC alarm peripheral could be used to determine the standby delay, a separate timer interrupt would need to be used to regularly update the time remaining on the LCD.

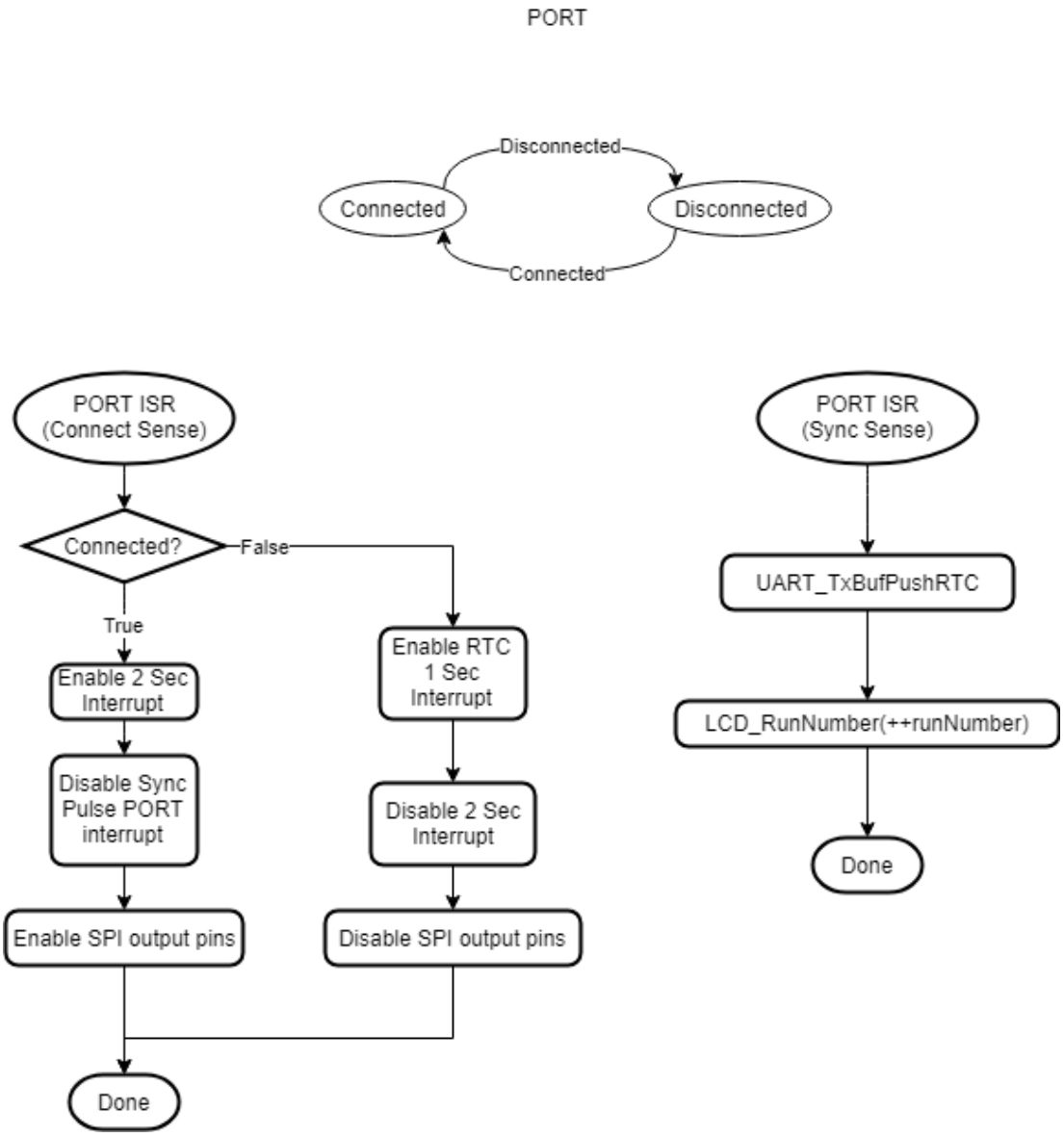


Figure 76: Detailed State Diagram and Flow Chart of Port (Source Monitor Unit)

When the devices are connected, the charge status interval timer is enabled, the sync pulse detect interrupt is disabled, and the SPI output pins are enabled. When the devices are disconnected, the standby timer is enabled, the charge status timer is disabled, and the SPI output pins are disabled so that when the devices are reconnected, the detector has time to reconfigure its SPI peripheral as a slave to prevent to outputs driving the bus. The sweep sync pulse from the signal generator will trigger an interrupt that pushes the current RTC value into the UART transmit buffer and updates the run number on the LCD.

B 7. Prototyping Progress Report

Components Acquired:

- NLB-300 Broadband RF Amplifier
- TCBT-14+ Wideband RF Bias Tee
- 1602 LCD
- MSP430F5529
- MSP430FR6989
- RO4350B PCB substrate

Components Awaiting Delivery:

- ADL5906 Evaluation Board

Prototyping in progress:

1) Parallel data interface with LCD display for source monitor:

- Modifying the libraries provided by the University of Texas El Paso for compatibility with the MSP430F5529 (PORT assignments, processor clock speed, etc.)
- Ensure the 1602 LCD works with the microcontroller before assembling the source monitor
- Complete

2) Writing data to SD card via Serial Peripheral Interface (SPI):

- Ensure that our system is able to record data smoothly at the rate in which we are collecting data
- Modifying the libraries provided by Texas Instruments for compatibility with the MSP430F5529 and MSP430FR6989 (SPI peripheral configurations, slave select PORT configuration, etc.)
- Modifying the libraries provided by Texas Instruments for compatibility with newer high capacity SD cards (initialization command sequence changes)
- Using SD card breakout on TFT LCD display board and libraries provide by Texas Instruments and application note SLAA281C
- Complete

3) Using emulated COM port for UART communication between MSP430F5529 and computer

- Using the Simple USB Back Channel libraries provided by Texas Instruments
- Complete

4) Integrating separate functioning software components into single project:

- Deconflict initialization differences between stand-alone software components. For example, the software for interfacing with the SD card runs the system clock at 8 MHz instead of the default 1 MHz for faster data transfer. So, the LCD software needed to be modified to function with an 8 MHz clock, as the display has a time sensitive communication protocol
- Reverify the operation all peripheral functionality as each new component is integrated and debug as necessary
- Complete for MSP430F5529 (behavioral interaction of software components in progress)

- In progress for MSP430FR6989

5) Measuring ADL5906 performance on evaluation board:
   - Input known RF signals into the device to ensure the ADL5906 will meet our requirements and work as expected within our system.
   - Awaiting ADL5906 evaluation board delivery

6) Low-frequency model of RF front-end to develop software behavior:
   - Ensuring that the software is behaving as expected without having to deal with RF signals will allow us to troubleshoot any early problems with the microcontroller. The low-frequency model will allow this troubleshooting to be done with more readily available signal generators, like the ones at GMU.
   - In progress.

7) Measuring NLB 300 performance:
   - Input known RF signal into the device to ensure increased detectable power for the detector.
   - Simulation based on NLB 300 datasheet is performed in MATLAB
     - Random RF signal is generated over the frequency range of 0.1 to 6 GHz with maximum power of 0.001mW and minimum power of 0 as shown in Figure 39. These values are chosen corresponding to the minimum detectable power of -30dBm, which translates to 1µW.

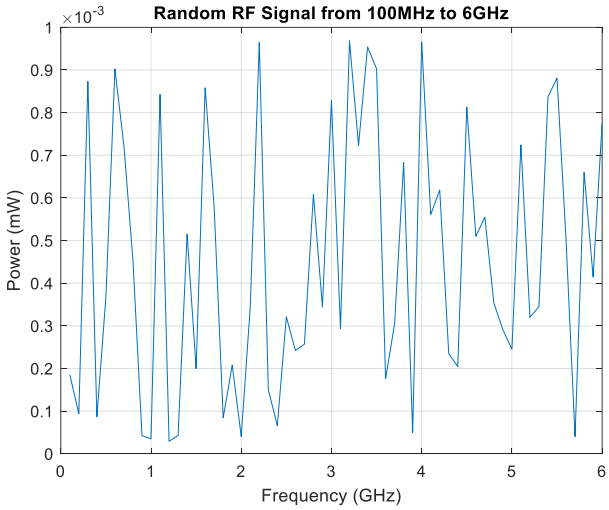


Figure 77: Random RF Signal from 100MHz to 6GHz

Since the simulated signal is below the minimum threshold of -30 dBm, it will not be detectable by the detector in its original state.

- Theoretical amplifier gain response over the frequency range is generated based on the datasheet, Table 1, and the experimental response found on the datasheet is generated as well to give Figure 40.

Table 1 [4]

Frequency (GHz)	Average Gain (dB)
0.1 ~ 1.0	13.0
1.0 ~ 4.0	10.7
4.0 ~ 6.0	8.9

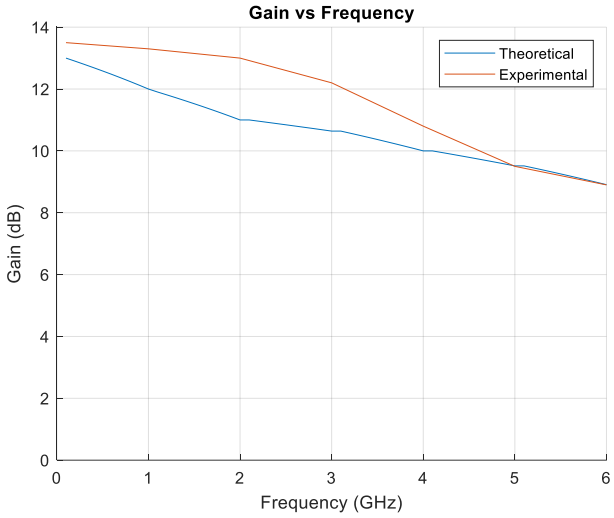


Figure 78: Gain vs Frequency Characteristic of Amplifier

- Based on the theoretical gain response, amplified signal is generated as displayed in Figure 41.

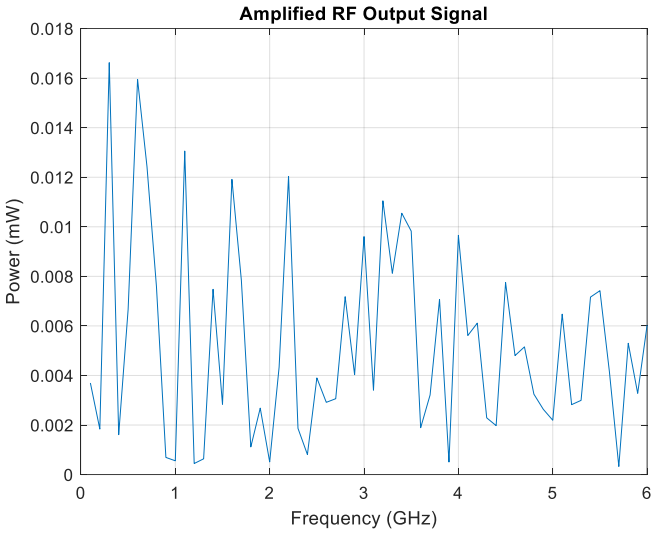


Figure 79: Amplified RF Signal

There is significant increase in signal strength overall. The gain becomes less effective as frequency increases, but the amplification is still significant as shown in Figure 42, displaying both the original and the amplified signal.

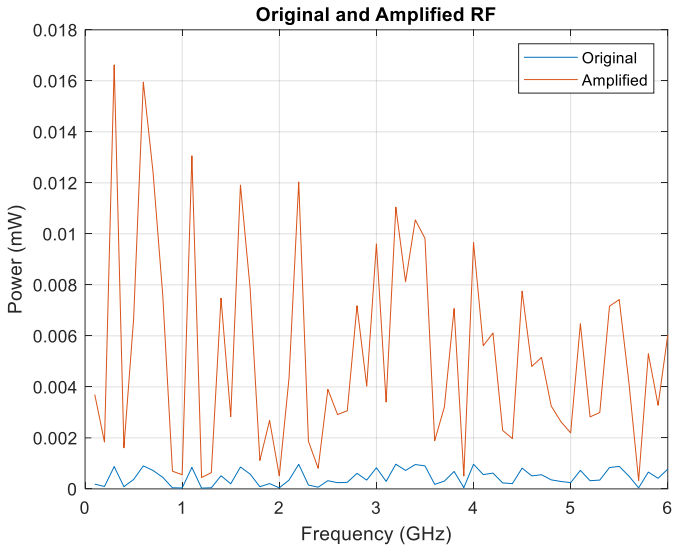


Figure 80: Original and Amplifier RF Signals

- The effect of the amplifier is more evident in dBm plot exhibited in Figure 43.

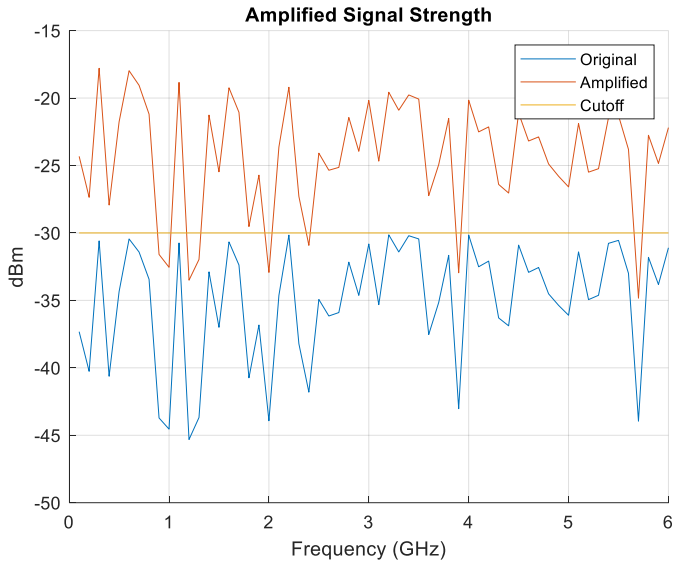


Figure 81: RF Signal Strengths of Original and Amplified

While the original signal is below the -30 dBm line, the minimum detectable power range, the amplified signal is mostly above the threshold.

Note: Due to the nature of our project, and the care that must be taken with RF/Microwave signals, we have elected to spend more time reading datasheets and planning the circuit than prototyping thus far.

B 8. Testing Plan

Experiment #1

- Goal: To evaluate Real Time Clock (RTC) synchronization
- System components: MSP430 in both detector unit and source monitor unit with source computer
- Testing process:
    - The microprocessors will be connected to connected to each other as well as the source computer and then the RTC will be synchronized
    - Time delay portion will be set to a value and be synchronized as well
    - With detector unit detached, the units will be given time longer than time delay
    - At least three testing shall be done with one test lasting for 8 hours
- Data collection:
    - The time delay start-up on the detector unit will be observed as well as its synchronization with the source monitor unit
    - RTC of both units
- Evaluation:
    - The time delay startup should be same for both units as well as the source computer. Any difference should be noted
    - The RTC of both units should have no difference between each other and with the source computer

Experiment #2

- Goal: To evaluate the minimum detectable power and dynamic range over the frequency range of operation
- System components: RF input SMA, RF detector, amplifier, measuring device
- Testing process:
    - With RF source directly connected to RF input SMA, RF source will do a sweep
    - From minimum RF of 100 MHz to maximum RF of 6 GHz range will be ran with known power values
    - The values of RF power will be varied: power ranging from below 1 µW and above
    - Experiments will include power of 500 µW, 1 µW, 0.5 µW, and any additional intermediate values as seem fit
- Data collection:
    - The detected power corresponding to each RF will be recorded
- Evaluation:
    - Compare the recorded data with the known power of the RF that was emitted at corresponding time, which should be with accuracy of ± 2 dB
    - The recorded data should have been able to record corresponding RF at specific frequencies, which would indicate the correctly working detection
    - Amplification of detected RF and range of detected RF should meet the requirement of 100 MHz to 6 GHz with 0 to -30 dBm

Experiment #3

- Goal: To evaluate the life span of battery power
- System components: RF input SMA, Battery, RF detector, amplifier, battery life indicator, measuring device
- Testing process:
    - Simple version of this testing for general life span of battery life will be to create a required constant stream of power for the detector unit
    - Alternative and more precise method is to have the battery connected to the detector unit with constant power and constant frequency RF input and allow it to run it until the power runs out
    - At least two testing shall be done
- Data collection:
    - The time it takes for the battery life indicator to go down to 0 or diminished power from the requirement to power up the detector unit will be recorded
    - The constant power and constant frequency RF will be recorded
- Evaluation:
    - The battery life will be indicated by the diminished power of the RF for fully functional operation of the detector unit
    - The time will be measured from the moment power is supplies to the moment power supply is below the threshold or required power for the unit
    - Battery life should be minimum of 8 hours with accurate reading of RF power

Experiment #4

- Goal: To evaluate the sampling rate and data storage
- System components: SD card, RF input SMA, detector, MSP430
- Testing process:
    - Any ranges of RF will be fed into the detector via SMA and will be sampled to be put into the SD card or data storage over time
    - One test should be sufficient
- Data collection:
    - Sampled data will be stored in data storage
    - Time shall be recorded
- Evaluation:
    - Analyze how many samples are being collected per second to calculate the rate, which should be greater than 230 samples per second
    - Data storage limit should have minimum of 7 million samples

Experiment #5

- Goal: To evaluate susceptibility of detector unit circuit to RF
- System components: detector unit
- Testing process:
    - RTC synchronization

    - With the RF input terminated, the detector unit will be placed inside stirred-chamber
    - Detector unit will be exposed to known RF sweep
    - At least two testing shall be done
- Data collection:
    - The RF will be detected with power recorded
    - RTC
- Evaluation:
    - Check to see if there is lost synchronization of RTC (between the detector unit and source monitor unit)
    - Check the data gathered and compare to the RF sweep done to see if there is any disparity in recorded data or erroneous reading
    - Check the amplification and detected frequency range to see if there is any difference compared with when the detector unit is not exposed to the stirred-chamber directly

B 9. Tasks for ECE 493

B 9.1 List of Major Tasks

1. **Hardware development** (6 weeks)
    - 1.1 RF detector setup
        - Selecting detector component that can be best integrated into the system with meeting the required detection RF range and power output.
        - Testing and analyzing performance.
    - 1.2 Amplifying stages setup
        - Identifying needed amplifying stages and selecting component that can achieve specific goals of amplification and be implemented into the system.
        - Testing and analyzing performance.
    - 1.3 Circuit design
        - Integrating different components into one circuit design.
        - Incorporation microcontroller to the circuit design.
        - Calculating correct resistor, capacitor, inductor, or any elements in need's values to complete the design.
    - 1.4 ADC process
        - Overseeing analog wave to DC to digital bit conversion process and analyzing resolution to fit the need.
    - 1.5 Connection ports setup
        - The input and output setup of the hardware.
        - Antenna SMA front end with data output link on the back end for the detector unit.
        - Source monitor unit has connection to the computer as well as to the detector unit: USB port, SUB-D9, and BNC.
    - 1.6 PCB design
        - Designing traces, especially for RF transmission line, and incorporating circuit design layout onto the PCB design.
    - 1.7 PCB assembly
        - Cutting of the board to the specification of the design and incorporating all the components on it.
2. **Power supply development** (3 weeks)
    - 2.1 Battery power design
        - Selection of efficient battery that can provide necessary voltage and current.
        - Calculation of those necessities and life span.
    - 2.2 Power connection setup
        - Power distribution setup to necessary components and implementation to the PCB design.

- Power connections among detector unit, source monitor unit, and source computer.

2.3 Power charging setup

- Wire connection from detector to source monitor that will charge the battery as well as indication of battery life.

3. Software development (6 weeks)

3.1 RTC module

- Setting up RTC and synchronization among the units which includes timestamping and time delay initiation.

3.2 Data storage module

- Storing digitized information of the RF power into data storage, SD card.
- Storing timestamping or RTC information.
- Management of data.

3.3 Power management module

- Controlling power distribution among components, shutting down when not necessary to conserve power.
- Detection of power level.

3.4 Initiation module

- With time delay, synchronize the power distribution to necessary components as initiation of testing sequence.

3.5 Pass thru/connection module

- Being able to efficiently relay information among the units.
- Passing data storage information from detector unit to source monitor unit to source computer. Connection, USB, port usability on the source monitor unit

3.6 LED display module

- Displaying relevant information according to the design on LED screen.

3.7 Sweep number sync module

- Enable source monitor unit to keep track of sweep pulse number for analysis after the test.

4. System integration (4 weeks)

4.1 PCB and microcontroller integration

- Integrating all necessary components onto PCB and create detector unit and source monitor unit.

4.2 System configuration module

- Synchronization and configuration capabilities from the source computer and its corresponding program.

4.3 Display functionality

- LED display relaying accurate reading and information.

4.4 Connection functionality

- Connecting all the units and test for proper functionalities.
- After proper disconnection, test for proper functionalities of the units.

5. **Testing** (4 weeks)
    5.1 Experiment #1
        - Evaluate RTC synchronization
    5.2 Experiment #2
        - Evaluate minimum detectable power and dynamic range
    5.3 Experiment #3
        - Evaluate battery life span
    5.4 Experiment #4
        - Evaluate sampling rate and data storage
    5.5 Experiment #5
        - Evaluate susceptibility of detector unit to RF
6. **Reporting**
    6.1 Progress report
    6.2 In-progress presentation
    6.3 Final report
    6.4 Final presentation
7. **Milestones/Demos**
    7.1 Demo #1
        - Circuit board functionality demonstration
        - Microcontroller functionality demonstration
    7.2 Demo #2
        - Functionality of detector unit and monitor unit demonstration
    7.3 Demo #3
        - Experimental results demonstration

B 9.2 Allocation of Responsibilities

There are two major modules for our design: hardware and software, and therefore, two teams composed of two members will be formed to oversee the production of each.

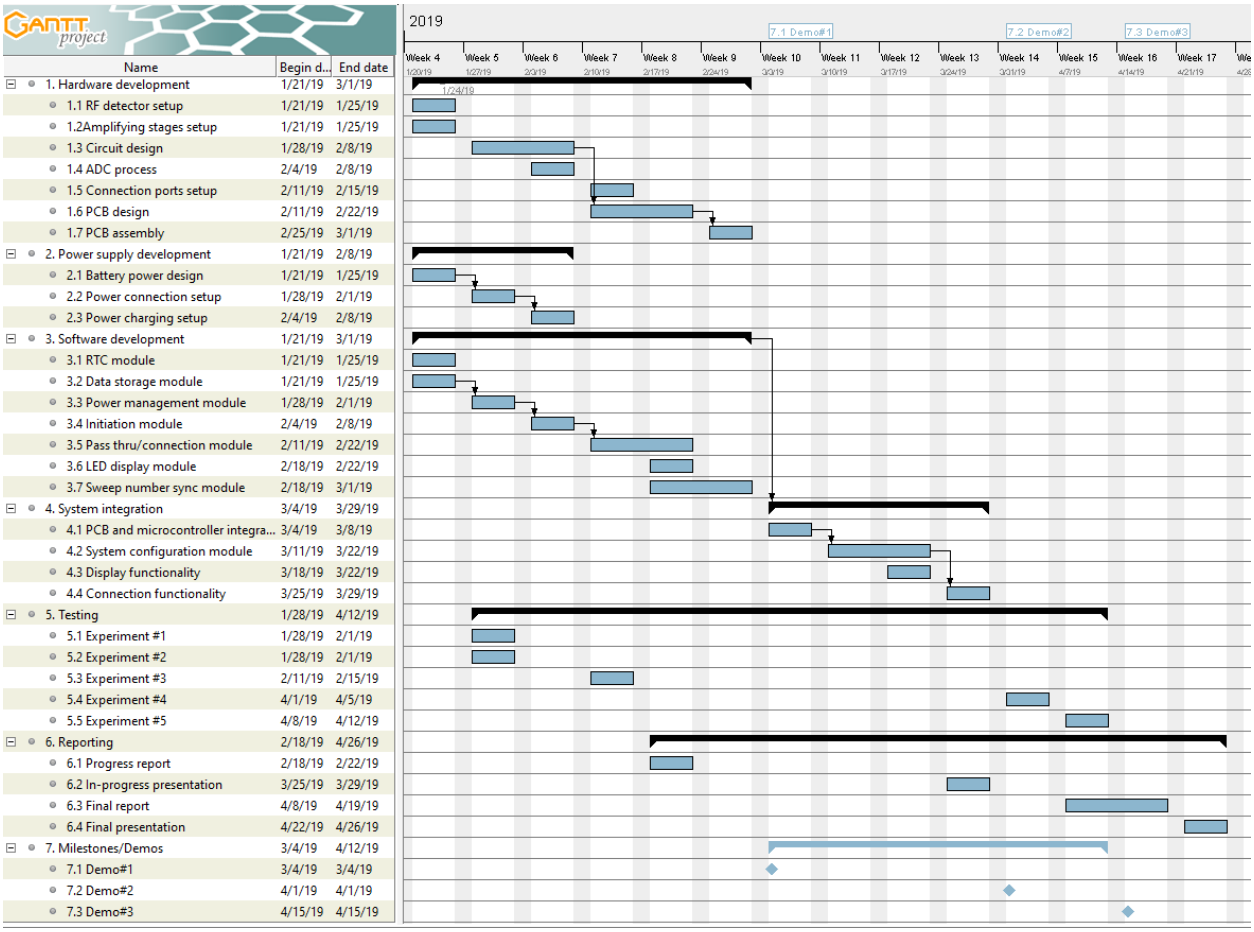
David Phelps and Steve Kim are tasked with hardware development including power module and part of system integration. This team is responsible for task #1 and #2, with David Phelps focusing on PCB design and power supply development and Steve Kim focusing on circuit design, component setups, and assembly.

Kevin Riley and Shahed Afrad team are tasked with software development. They are responsible for task # 3 and task #4, with task #4 shared with the other team with hardware integration. Kevin Riley will focus on software development of detector unit, and Shahed Afrad will focus on software development of source monitor unit.

Tasks #5, 6, and 7 will be distributed accordingly to modules.

Kevin Riley has the responsibility of project manager who will oversee the progress of the tasks and the project to keep the team focused on the objectives. Clear organization and communication will be vital for the success of the project, and each member will help one another as needed.

B 10. Schedule



Name	Begin d...	End date
1. Hardware development	1/21/19	3/1/19
1.1 RF detector setup	1/21/19	1/25/19
1.2Amplifying stages setup	1/21/19	1/25/19
1.3 Circuit design	1/28/19	2/8/19
1.4 ADC process	2/4/19	2/8/19
1.5 Connection ports setup	2/11/19	2/15/19
1.6 PCB design	2/11/19	2/22/19
1.7 PCB assembly	2/25/19	3/1/19
2. Power supply development	1/21/19	2/8/19
2.1 Battery power design	1/21/19	1/25/19
2.2 Power connection setup	1/28/19	2/1/19
2.3 Power charging setup	2/4/19	2/8/19
3. Software development	1/21/19	3/1/19
3.1 RTC module	1/21/19	1/25/19
3.2 Data storage module	1/21/19	1/25/19
3.3 Power management module	1/28/19	2/1/19
3.4 Initiation module	2/4/19	2/8/19
3.5 Pass thru/connection module	2/11/19	2/22/19
3.6 LED display module	2/18/19	2/22/19
3.7 Sweep number sync module	2/18/19	3/1/19
4. System integration	3/4/19	3/29/19
4.1 PCB and microcontroller integra...	3/4/19	3/8/19
4.2 System configuration module	3/11/19	3/22/19
4.3 Display functionality	3/18/19	3/22/19
4.4 Connection functionality	3/25/19	3/29/19
5. Testing	1/28/19	4/12/19
5.1 Experiment #1	1/28/19	2/1/19
5.2 Experiment #2	1/28/19	2/1/19
5.3 Experiment #3	2/11/19	2/15/19
5.4 Experiment #4	4/1/19	4/5/19
5.5 Experiment #5	4/8/19	4/12/19
6. Reporting	2/18/19	4/26/19
6.1 Progress report	2/18/19	2/22/19
6.2 In-progress presentation	3/25/19	3/29/19
6.3 Final report	4/8/19	4/19/19
6.4 Final presentation	4/22/19	4/26/19
7. Milestones/Demos	3/4/19	4/12/19
7.1 Demo#1	3/4/19	3/4/19
7.2 Demo#2	4/1/19	4/1/19
7.3 Demo#3	4/15/19	4/15/19

Figure 82: Schedule of Tasks for ECE 493

B 11. References

[1] C. K. Alexander and M. N. O. Sadiku, *Fundamentals of Electric Circuits*, 5th ed. New York, NY: McGraw-Hill, 2013.

[2] Mantaro, "Impedance Calculators," mantaro.com. [Online], Available: http://mantaro.com/resources/impedance-calculator.htm. [Accessed Nov. 15, 2018].

[3] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. New York; Oxford: Oxford University Press, 2015.

[4] RF Micro Devices Inc, *NLB-300 Datasheet (DS131015)*, Greensboro, NC, 2013.

[5] W. Stallings, *Data and Computer Communications*, 10th ed. Boston: Pearson, 2014.

[6] Analog Devices Inc., *ADL5906 Datasheet Rev. A*, Norwood, MA, 2013.