ABIRAMI PRABHAKARAN
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WORK EXPERIENCE

Component Design Engineer, Intel, Jones Farm Campus, Hillsboro, OR Present
Current work is to analyze and develop workloads for the server and client side of Hetero core processors to show the value proposition. Responsibilities also include benchmarking, power architecture design and measurements.

Computer Engineering Intern, Intel, Jones Farm Campus, Hillsboro, OR 06/10-12/10
Responsibilities included performance engineering work and benchmarking on the server systems being built that contain heterogeneous cores at the system and software stack level and doing power architecture work and measurements.

Graduate Researcher, Cryptographic Engineering Research Group, Fairfax, VA 08/09-05/11

- Research interests include power analysis attack on SASEBO-GII to reveal the key for block ciphers.
- As part of the voluntary research working on ATHENa, a Perl-script based automated evaluation tool which synthesizes and implements functions in VHDL, and produces results which are stored in a database. Responsibilities include testing ATHENa for bugs and analyze the results produced.

Teaching Assistant, George Mason University, Fairfax, VA Fall 2009-Summer 2010
Courses: Microprocessors, Computer Organization, Electric Circuit Analysis, Fundamentals of Engineering.
Responsibilities include: conducting lab sessions, grading homework and exams and prepare question papers for Undergraduate class. Help students with hands-on lab session on projects.

Technical Administrator, George Mason University, Fairfax, VA Aug 2008 – July 2009

- Complete software installs (MS Office, Adobe products), troubleshooting on Windows XP based systems (including imaging, wireless access and network printing issues) and configuration of workstations.
- Performing RAM installations, hardware diagnosis, troubleshooting and component repair on Dell, HP, Gateway, SONY VAIO, Apple PowerBook G4/G5 laptops and Desktops.

Trainee Engineer, BSNL, India June, 2006
Worked during a period of 1 month with Bharat Sanchar Nigham Limited, India to design probe line and RF based transmission line which communicates along 400 miles.

ADDITIONAL SELECTED EXPERIENCE

- Programming skills in VHDL gained by implementing projects like Tiger Hash Function, System Generator and Accel DSP, block ciphers targeting onto FPGA devices.
- Extensive debugging skills obtained from creating test benches to simulate digital circuits using VHDL and analyzing timing level simulations.
- Skilled in Matlab programming, achieved by writing scripts to perform Fuzzy logic Analysis of IPS system, and various other projects.
- Good programming skills in C and C#.

TECHNICAL SKILLS

Programmable Hardware	Xilinx FPGA and Altera FPGA
Programming Languages	VHDL, Verilog, MATLAB, C, C#, PSpice
Tools	Xilinx ISE, Xilinx System Generator and Accel DSP, ModelSim, Altera Quartus II, Active HDL, Simulink, Cryptool, Kryptos
Applications	HTML, Microsoft Visio, Open office, MS Office, LaTeX
Operating Systems	Windows, Mac OS X, GNU/Linux

PROJECTS AND PRESENTATIONS

- **Benchmarking of secret key block cipher modules using ATHENa** Fall 2009
  This project involved using a GMU based benchmarking tool ATHENa, to obtain the implementation results for the secret key block cipher modules chosen: DES, 3DES, TWOFISH, BLOWFISH, MARS, and SERPENT.
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- **Parallelizing an application onto a multicore platform using MPA tool** Fall 2009
  A term paper presentation shows how an application like MPEG-4 encoder can be parallelized onto a multicore platform using an MPA tool.

- **Implementation of adder circuits using Xilinx System Generator and AccelDSP** Spring 2009
  Final project involving synthesizing and implementing Tiger hash function on System Generator and AccelDSP. This project also involved simulation in Simulink and comparing the outputs from Synthesis in Xilinx.

- **Temperature variation characterization of multicore architectures** Spring 2009
  A term paper presentation under the guidance of Dr.Tabak shows how temperature variations affect multicore architectures and thermal management techniques to prevent it.

- Design project on **"CMOS inverters"** and **"Two stage operational amplifiers"** using PSpice in spring 2009 and fall 2008 respectively.

- **Design project on "Implementation of Tiger hash function"** Fall 2008
  Complete synthesis and implementation of Tiger Hash function on Xilinx Virtex family.

- **A term paper on AMBRIC's programming model & Hardware Architecture** Fall 2008

- **"Double Level Modular Fuzzy Logic Controller using Genetic Algorithms"** presented under the guidance of Mr. P.V.Sunil Nag, M.Tech, at Amrita School of Engineering, India. This project involves designing an Inverted Pendulum System using Fuzzy Logic Controller and control the functioning of the pendulum using Genetic Algorithms.

RELEVANT COURSE WORK

Graduate: Microprocessors, Advanced Microprocessors, Computer systems Architecture, Design Analog Integrated Circuits, Digital Integrated Circuits-CMOS technology, Digital System Design w/ VHDL, Cryptography and Network security, Digital Signal Processing and Hardware Implementations.

Under-Graduate: Electric Circuit Theory, Electronic Circuits & Devices, Digital Design, Signals & Systems, Control Engineering, Sensors & Transducers, Microcontrollers, Intelligent Systems & Automation, Digital Signal Processing, Power Electronics, Biomedical Instrumentation & Measurements, Process Control Instrumentation, Analytical Instrumentation, VLSI Technology, VLSI Design, Introduction to Soft Computing.

EDUCATION

M.S., Computer Engineering, George Mason University, Fairfax, VA May 2011
Thesis: Side-channel Analysis of Block Ciphers using CERG-GMU interface on SASEBO-GII

B.S., Electronics and Instrumentation Engineering, May 2008
Amrita School of Engineering, Tamilnadu, India

OTHER INFORMATION

Member, Cryptographic Engineering Research Group, George Mason University, August 2009-May 2011.

REFERENCE

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